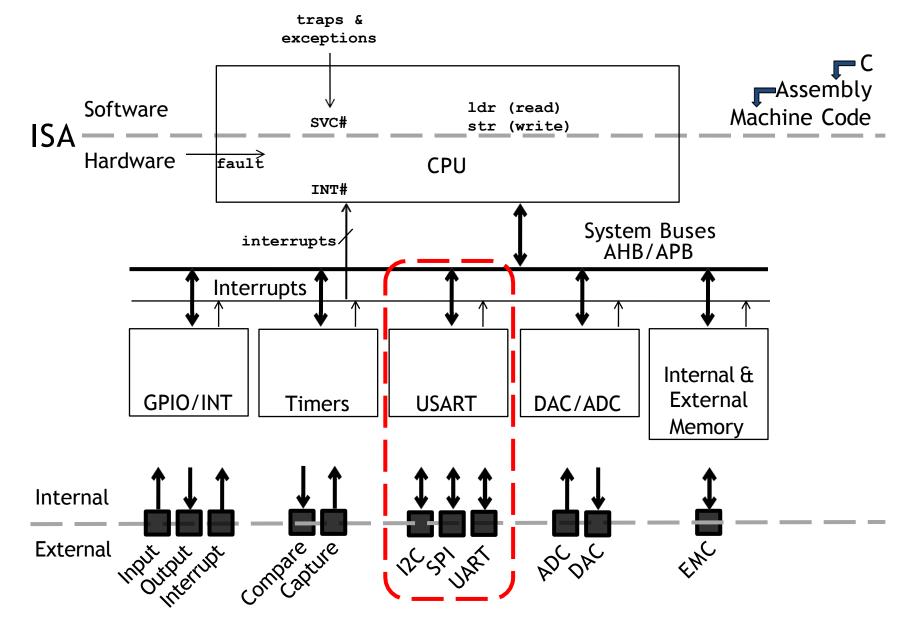
Serial Buses

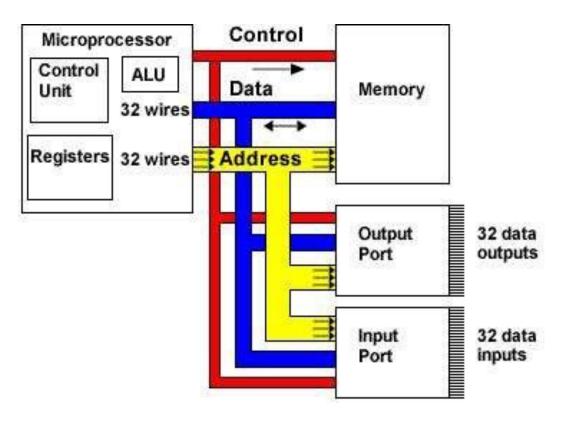
- · USART
- I²C
- · SPI
- ADCs and DACs
- · Operation

Serial interfaces



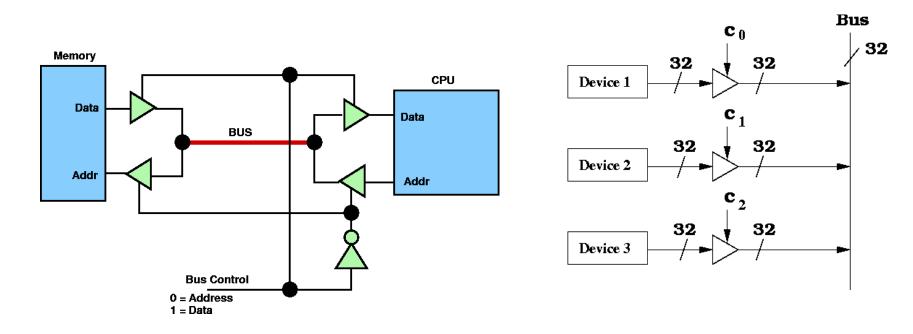
Bus organization

- Multidrop bus (MDB): components on same wires
- More than one component can drive
- Might be multi-master



Review: Multiple (potential) bus drivers (1)

- Tri-state devices: one on at a time.
- All can read.
- Pin-efficient, low-power.
- Potentially dangerous.

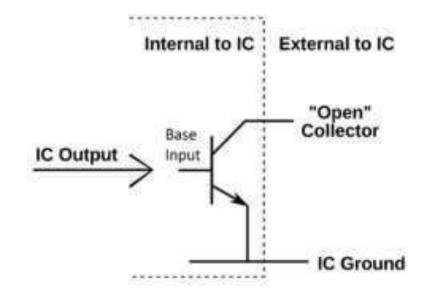


Review: Multiple (potential) bus drivers (2)

- MUX
 - Many pins.
 - Consider a 32-bit bus with 6 potential drivers.
 - Generally impractical on PCB.
 - More practical on-chip.

Review: Multiple (potential) bus drivers (3)

- "pull-up" aka "open collector" aka "wired OR"
- Pull high with resistor
- Any device can pull low
- Safe
- Fast or energy efficient, pick one
- Used in I²C, CAN



UART

- Universal Asynchronous Receiver/Transmitter
- Translates data between parallel and serial forms.
- UARTs used in conjunction with communication standards such as EIA, RS-232, RS-422 or RS-485.
- Universal
 - Configurable data format and speed.
 - Signaling levels/methods delegated.

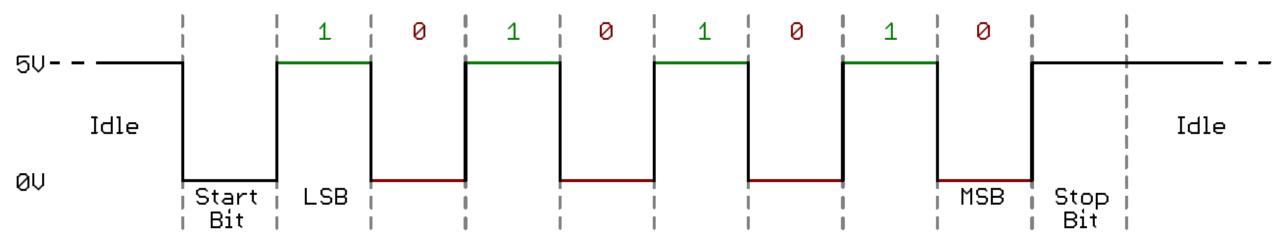
Protocol

• Each character is sent as

- a logic *low* start bit
- a configurable number of data bits (usually 7 or 8, sometimes 5)
- an optional **parity** bit
- one or more logic high stop bits with a particular bit timing ("baud" or "baudrate")
- Examples

<9600-N-8-1= <baudrate><parity><databits><stopbits>

<9600-8-N-1= <baudrate><databits><parity><stopbits>



Variations

- U(S)ART is actually a generic term that includes a large number of different devices/standards.
- RS-232 is a standard.
- Specifies characteristics and timing of signals, the meaning of signals, and the physical size and pin out of connectors.

Most commonly used signals

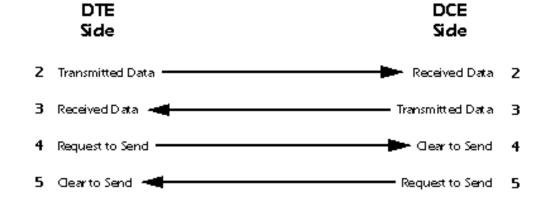
• Definitions

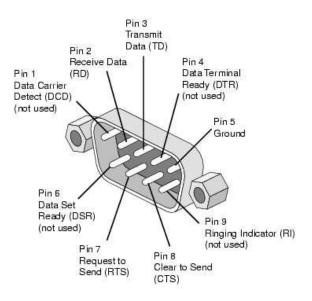
DTE: Data terminal equipment
DCE: Data circuit-terminating equipment **RXD**: for receiving data. **TXD**: for transmitting data

- Flow control.
 - RTS# (Request to Send): DTE calls for DCE to send data..
 - CTS# (Clear to Send): DCE tells DTE it is ready to accept data..
 - RXD TXD
 - RTS CTS

DB9 stuff

- DTE vs. DCE.
- Pinout of a DCE?
- Common ground?
- Noise effects?





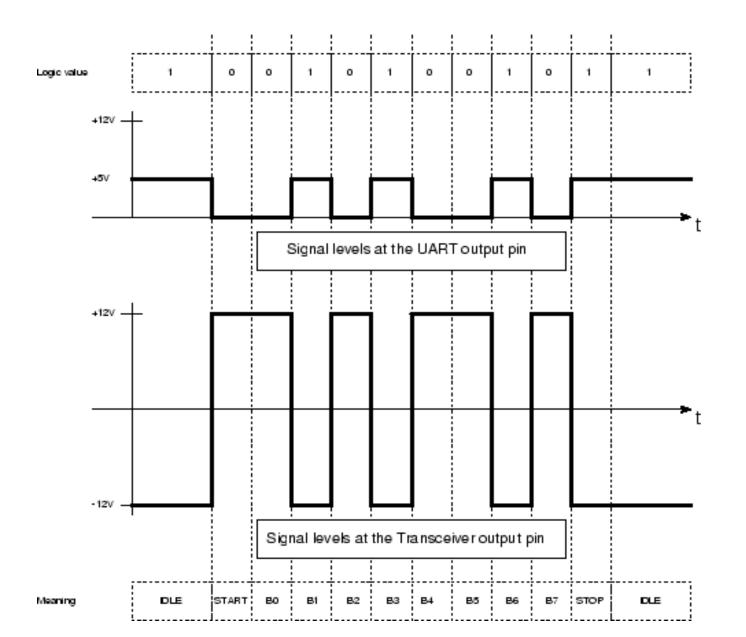
Pin Number	Signal	Description
1	DCD	Data carrier detect
2	RxD	Receive Data
3	TxD	Transmit Data
4	DTR	Data terminal ready
5	GND	Signal ground
6	DSR	Data set ready
7	RTS	Ready to send
8	CTS	Clear to send
9	RI	Ring Indicator

DTE DCE: wires connect pin x x.

DTE DTE: crossover or null modem cable needed.

RS-232 transmission example

RS232 Transmission of the letter 'J'



I²C summary

- Inter integrated circuit bus.
- Two-wire protocol.
- From Philips in early 1980s.

I²C applications

- Initially in TV sets.
- Common for peripherals from many companies.
- Real-time clocks.
- Temperature sensors.
- Many others.

I²C technical description

- Two-wire serial protocol.
- Addressing.
- Up to 3.4 Mb/s.
- Multi-master, multi-slave.

I²C wiring

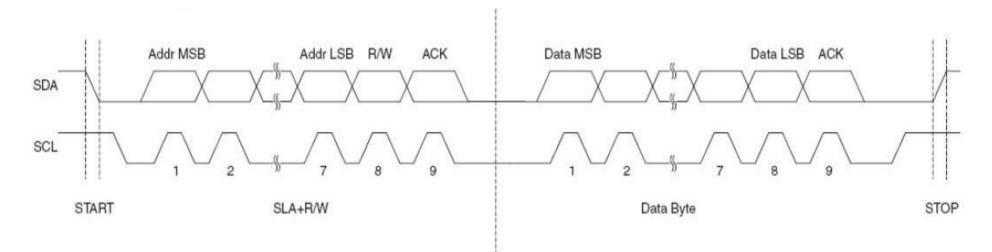
- SDA: data.
- SCL: clock.
- Open collector.
- Simple interfacing among voltage domains.

I²C clocking

- Unconventional.
- Quiescent state is high.
- Leader pulses low during transmission.
- Follower holds clock low to extend transmission cycle.
 - Open-collector design enables this.

I²C transaction

- Leader initiates.
- Start.
- Address.
- Data.
- Ack.
- Stop.



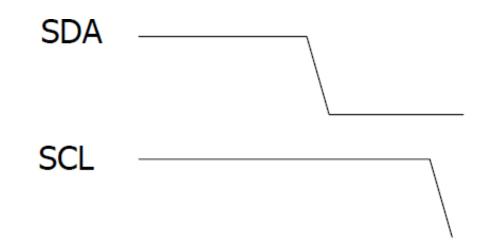
Source: ATMega8 Handbook

I²C roles

- Transmitter/receiver not same as master/slave.
- Leader initiates transactions.
- Transmitter sends data on SDA.
- Receiver acks.
- Read: follower is transmitter.
- Write: leader is transmitter.

I²C starting

- Leader drives SDA low while SCL remains high.
- During other parts of transactions, SDA changes when SCL is low.

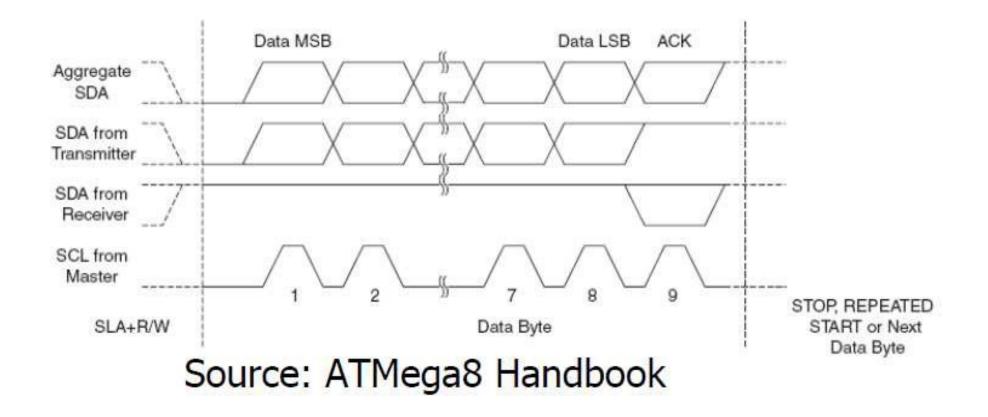


I²C address

- Sampled on rising SCL.
- 7-bit address.
- 8th bit
 - Low: write.
 - High: read.
- Philips/NXP can assign standard addresses for a fee.
- Devices with hard-coded addresses troublesome.
 - What if >1 device needed?
 - Segment bus?
 - Add select line outside bus protocol?
 - Add custom select/MUX circuitry?

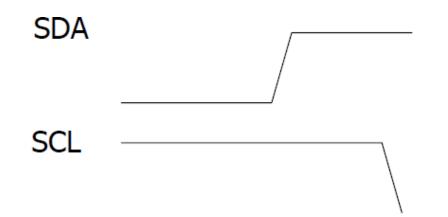
I²C data

- Sampled on rising SCL.
- 8-bit.
- Write: leader transmits, follower acks.
- Read: follower transmits, leader acks.
- Continues until leader signals to stop.

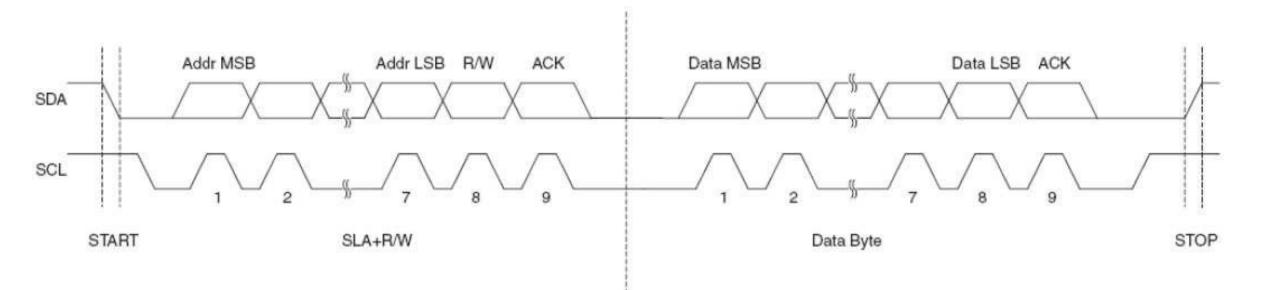


I²C stopping

- Leader allows SDA to go high while SCL high.
- Stops or aborts transactions.



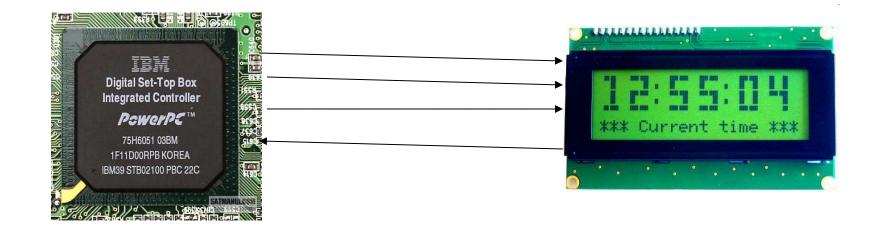
I²C timing diagram



Source: ATMega8 Handbook

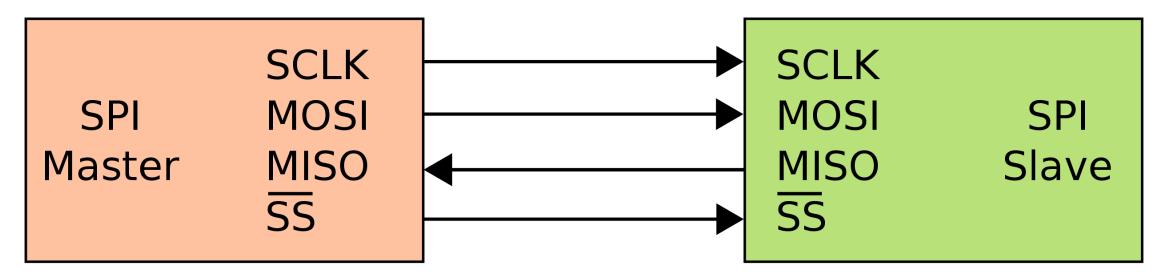
What is SPI?

- Serial bus protocol.
- Fast, easy to use, simple.
- Widely supported.



Introduction

- What is it?
- Basic Serial Peripheral Interface (SPI). Capabilities.
- Protocol.
- Pro / Cons and Competitor. Uses.
- Conclusion.



Serial Peripheral Interface

http://upload.wikimedia.org/wikipedia/commons/thumb/e/ed/ SPI_single_slave.svg/350px-SPI_single_slave.svg.png

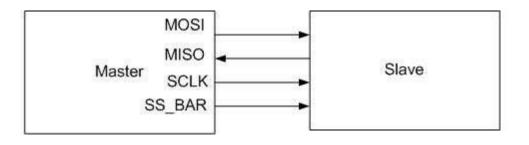
SPI basics

- 4-wire bus.
- Short-range.
- Multiple slaves, single master.
- Synchronous.

Capabilities of SPI

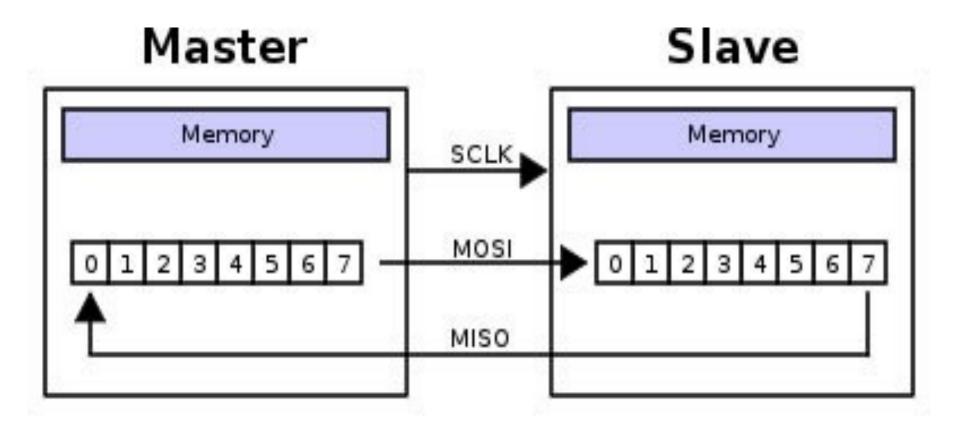
- Always full duplex.
 - Parallel bidirectional communication.
- Multiple Mb/s transmission speed.
- Transfers data in 4 to 16 bit characters.
- Multiple slaves.
 - Daisy-chaining possible.

Protocol



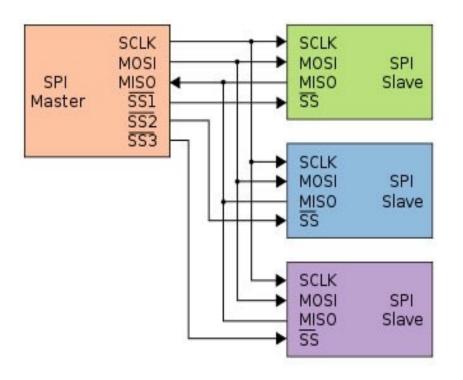
- Wires:
 - Master Out Slave In (MOSI).
 - Master In Slave Out (MISO).
 - System Clock (SCLK).
 - Slave Select (many of these).
 - Master sets SS low.
- Master generates SCLK.
- Shift registers shift in and out data.

Shifting protocol



Master shifts out data to Slave, and shift in data from Slave http://upload.wikimedia.org/wikipedia/commons/thumb/bb/SPI 8-bit circular transfer.svg/400px-SPI 8-bit circular transfer.svg.png

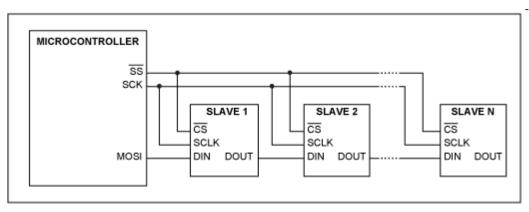
Diagram



Master and multiple independent slaves

http://upload.wikimedia.org/wikipedia/commons/thumb/f/fc/

SPI_three_slaves.svg/350px-SPI_three_slaves.svg.png



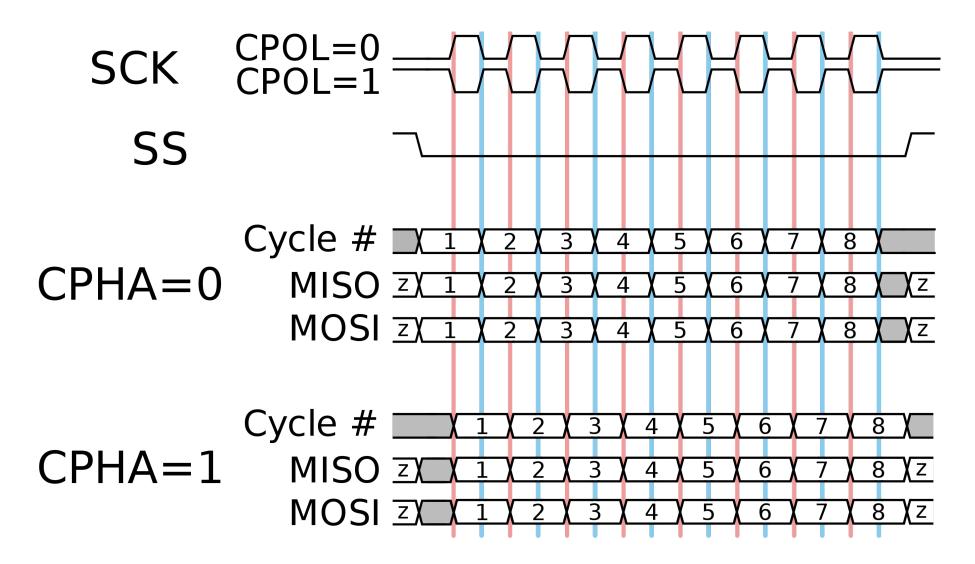
Some wires have been renamed

Master and multiple daisy- chained slaves

Clock phase (advanced)

- Two phases and two polarities of clock. Four modes.
- Master and selected slave must be in same mode.
- Master must change polarity and phase to communicate with slaves with different modes.
- Data transmission and latching happen on alternating clock edges.
- Why the complexity?
 - Increases peripheral implementation flexibility.

Timing Diagram



Timing Diagram 3 Showing Clock polarities and phases

Pros and cons

Pros:

- Fast and easy.
 - Fast for point-to-point connections.
 - Easily allows streaming / constant data innow.
 - No address bit / simple to implement.
- Full duplex.
- Widely supported.

Cons:

- SS signal makes multiple slaves wiring-intensive.
- No ack capability.
- No inherent arbitration.
- No now control.
- Four wires.

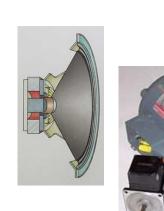
Summary

SPI 3 4 wire serial bus protocol

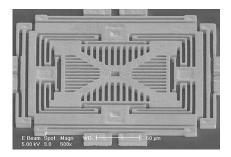
- MOSI MISO SS SCLK wires.
- Full duplex.
- Multiple slaves, one master.
- Best for point-to-point streaming data. Easily
- supported.

Many signals effectively analog

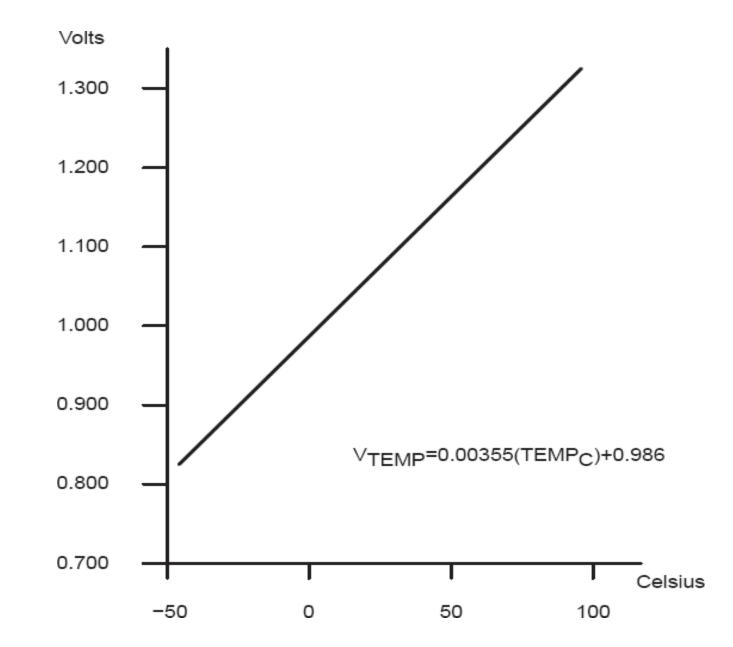
- Many signals are analog.
- Sound, light, temperature, pressure, voltage, etc.
- Path to digital system.
 - Source -> continuous voltage -> discrete value.
- Transducers: converts one type of energy to another
 - Electro-mechanical, optical, electrical
- Examples.
 - Microphone/speaker.
 - Thermocouples.
 - Accelerometers.







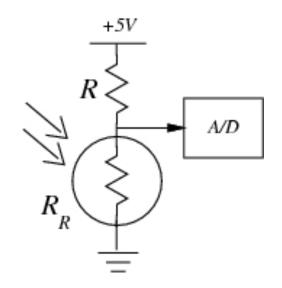
Transducers convert one form of energy into another



Convert light to voltage with a CdS photocell

• $V_{signal} = (+5V) R_R / (R + R_R).$

- Choose R=R_R at median of range.
- Cadmium Sulfide (CdS).
- Cheap, low current.
- $T_{RC} = (R+R_R) C_I$.
- Typically $R_R = 50-200$ kOhm
- C_I = 20 pF.
- So, T_{RC} = 20-80 us.
- $f_{RC} = 10-50 \text{ kHz}.$



Many other common sensors (some digital, 1/2)

- Force.
 - Strain gauges foil, conductive ink.
 - Conductive rubber.
 - Rheostatic nuids.
 - Piezorestive.
 - Piezoelectric films.
 - Capacitive force.
- Sound.
 - Microphones: current or charge.
 - Sonar: usually piezoelectric.
- Position.
 - Switches.
 - Shaft encoders.
 - Gyros.
- Atmospheric pressure.

Many other common sensors (some digital, 2/2)

- Acceleration
 - MEMS
 - Pendulum
- Monitoring
 - Battery energy
 - Motor velocity
 - Temperature
- Field
 - Antenna
 - Magnetic
 - Hall effect
 - Flux gate
- Location
 - Permittivity
 - Dielectric
- Conductivity
- Many, many more

Sensor strengths and weaknesses

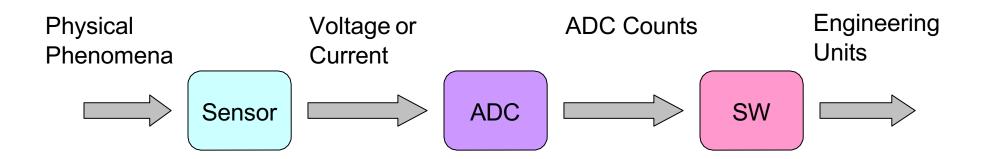
- Common for different sensors to provide information relevant to query of interest.
- Sensors generally perform well under some circumstances and poorly under others.
- E.g., cameras work well in daylight but not at night or in fog, sonar has different characteristics.
- Sensor fusion can cover more varied circumstances. Fusion of sensors that are all correlated to the query of interest but not correlated with each other can improve accuracy a lot.

Analog to digital

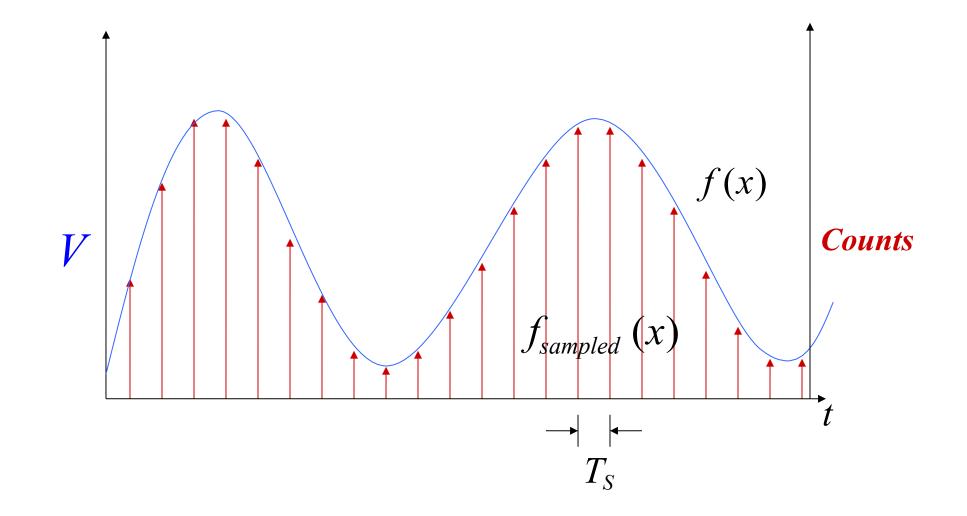
• Goal



• Process

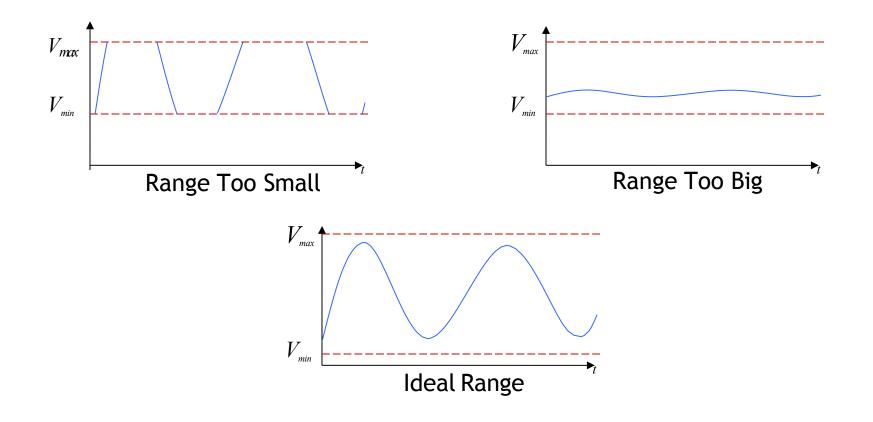


Digital representation of analog signal



Choosing the value range

- What do the sample values represent?
- Some fraction within the range of values

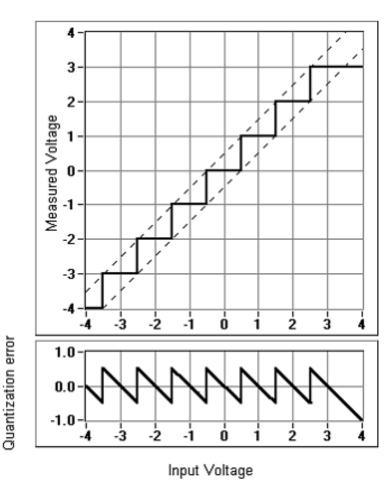


Choosing the value resolution

- Resolution
 - Number of discrete values that represent a range of analog values.
 - MSP430: 12-bit ADC
 - 4096 values
 - Range / 4096 = Step

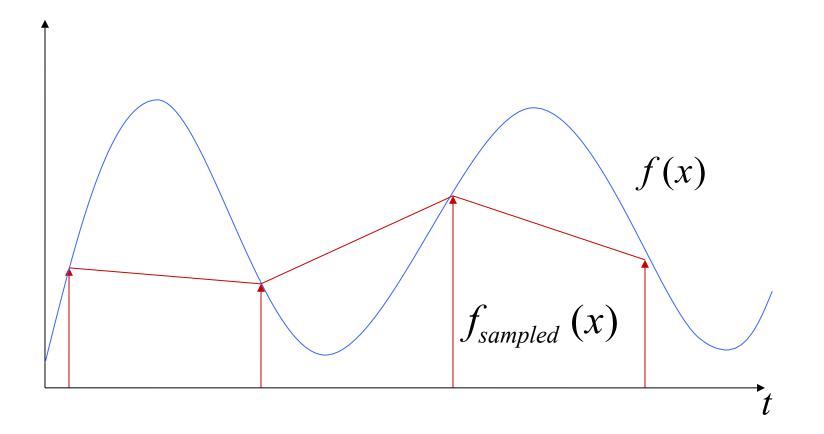
- Quantization Error
 - How far off discrete value is from actual
 - ½ LSB = Range / 8192

Larger range = lower resolution



Choosing the temporal resolution

Too low: we can't reconstruct the signal. Too high: waste computation, energy, resources.



Shannon-Nyquist sampling theorem

• If a continuous-time signal f(x) contains no frequencies higher than f_{max} , it can be completely determined by discrete samples taken at a rate:

$$f_{\rm samples} > 2 f_{\rm max}$$

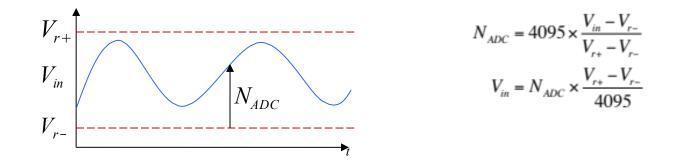
- Example:
 - Humans can process audio signals 20 Hz to 20 kHz.
 - Audio CDs: sampled at 44.1 Khz.
- Caveat: additional samples can have value if signal contains high-frequency noise.
 - Allows low-pass filtering. Improves accuracy.
 - Decreases effective samping rate.
 - Can sometimes fix with filter at measurement side.

Compressed sensing

- Can sometimes reconstruct well at below Nyquist rate.
- Relies on understanding (predictable) properties of signal.

Converting between voltages, ADC counts, and engineering units

• Converting: ADC counts to Voltage



• Converting: Voltage to Engineering Units

$$V_{\text{TEMP}} = 0.00355(\text{TEMP}_{\text{C}}) + 0.986$$
$$\text{TEMP}_{\text{C}} = \frac{V_{\text{TEMP}} - 0.986}{0.00355}$$

A note about sampling and arithmetic

• Common error converting values

$$V_{\text{TEMP}} = N_{ADC} \times \frac{V_{r_*} - V_{r_*}}{4095}$$
 TEMP_c = $\frac{V_{\text{TEMP}} - 0.986}{0.00355}$

volatile const int adccount;

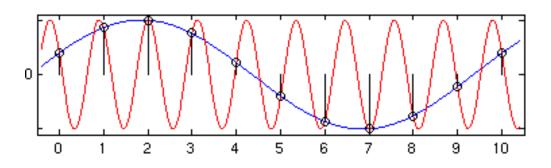
float vtemp = adccount / 4095 * 1.5;

float tempc = (vtemp-0.986) / 0.00355;

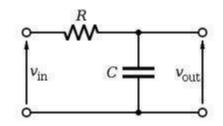
- Learn associativity and type conversion rules of ANSI C.
- Example.
- Fixed point operations
 - Overflow and underflow dangers complicate design.
 - Can use logarithmic representation for dynamic range.
- Floating point operations
 - Often software emulated.
 - Often slow, power-hungry on embedded processors.

Use anti-aliasing filters on ADC inputs to ensure that Shannon-Nyquist is satisfied

- Aliasing.
 - Different frequencies are indistinguishable when they are sampled.



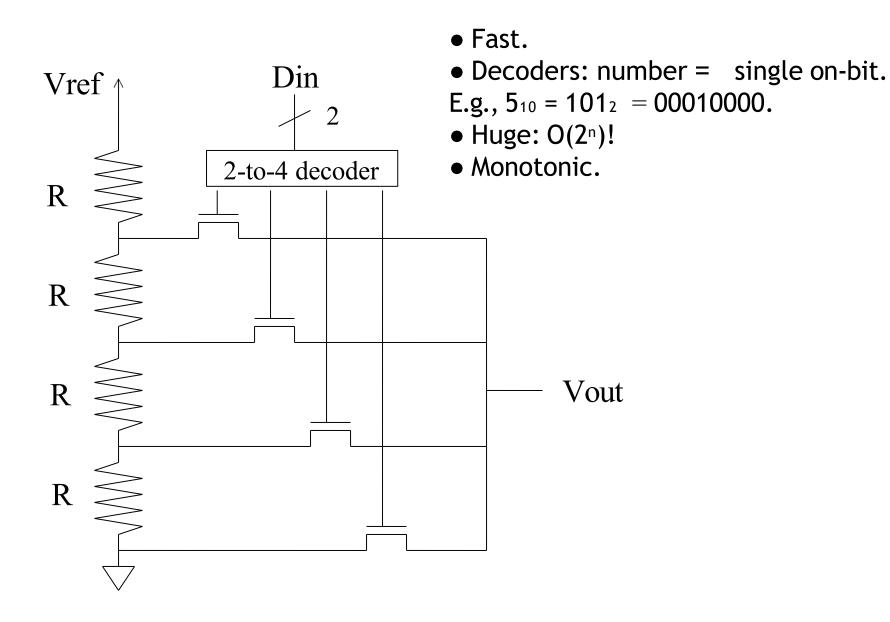
- Condition the input signal using a low-pass filter.
 - Removes high-frequency components.
 - A.K.A. anti-aliasing olter.



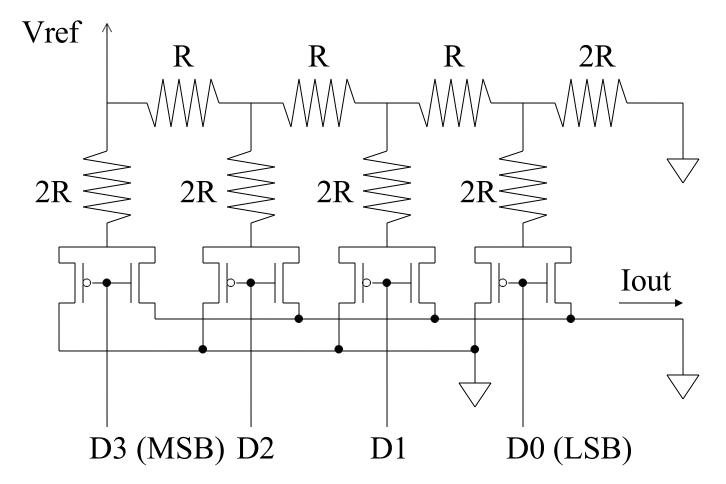
Do I really need to condition my input signal?

- Often.
- Many ADCs have analog olter built in.
- Those olters typically have a cut-off frequency just above ½ their *maximum* sampling rate.
- Which is great if you are using the maximum sampling rate, less useful if you are sampling at a slower rate.
- Can sometimes use random sampling phase offsets to avoid some aliasing problems.

DAC #1: voltage divider

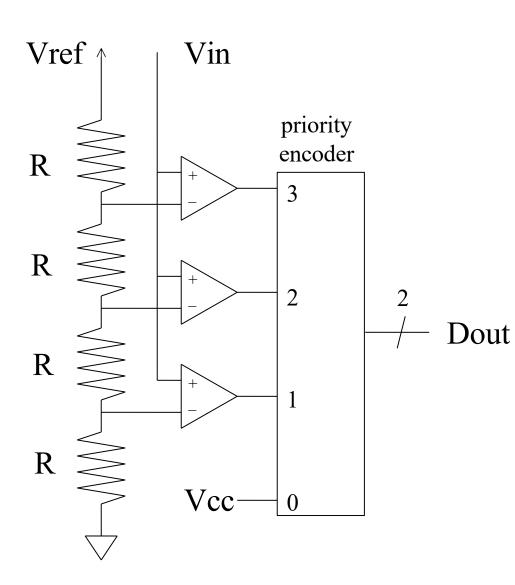


DAC #2: R/2R ladder



- Small: O(n).
- Monotonicity? (Consider 0111 -> 1000)

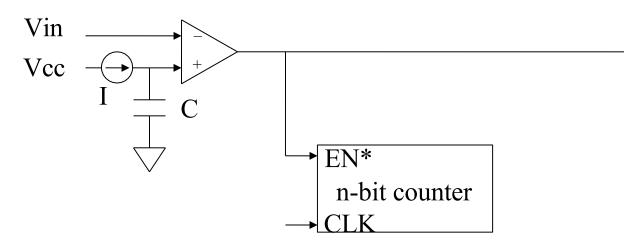
ADC #1: nash



- Compare input with linear range of voltages.
- Use priority encoder.
- Only leave on highest input bit.
 - 001111111³ 00100000.
- Convert input bit index to binary number.
- 00100000 ³ 110
 - Noting that 000000000 ³ 000.

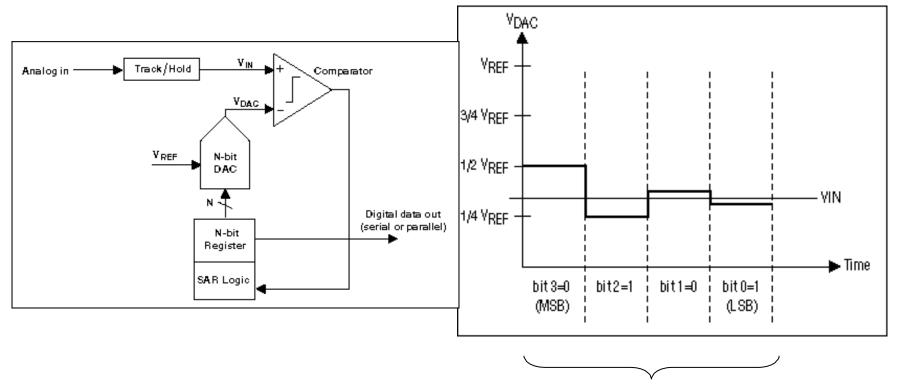
• Huge: O(2ⁿ).

ADC #2: single-slope integration



- Start: Reset counter, discharge C.
- Charge C at fixed current I until Vc > Vin.
- Final counter value is Dout.
- Slow: O(n^2).
 - Conversion may take several milliseconds.
- Good differential linearity (dI/dO).
- Absolute linearity depends on precision of C, I, and clock.

ADC #3: successive approximation

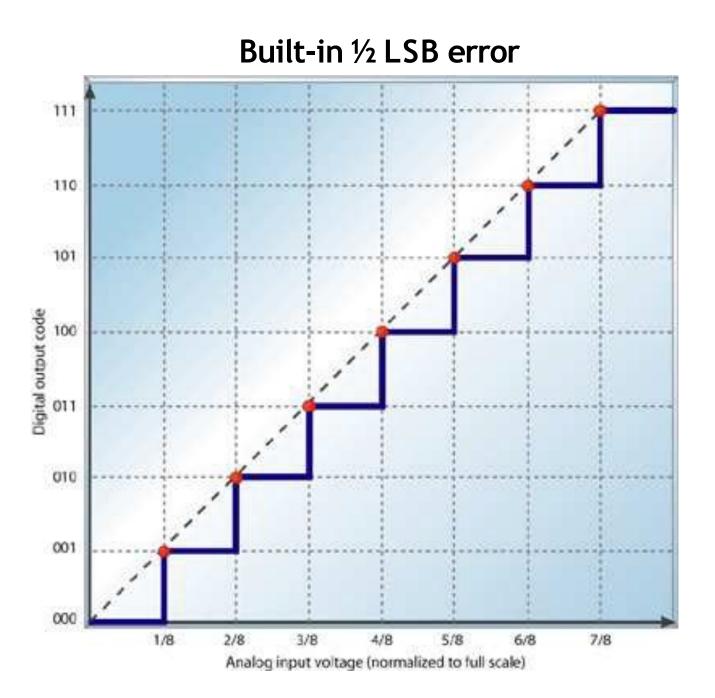


1 Sample = Multiple cycles

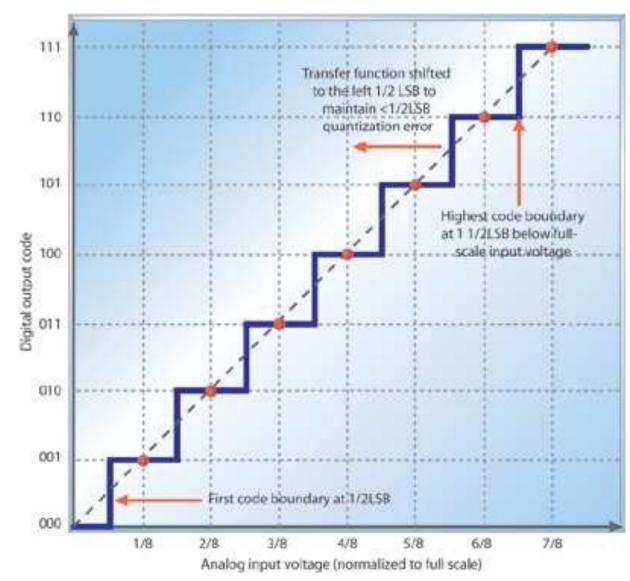
Uses DAC for guessing. Somewhat fast: O(n). Goes from MSB to LSB.

Errors and ADCs

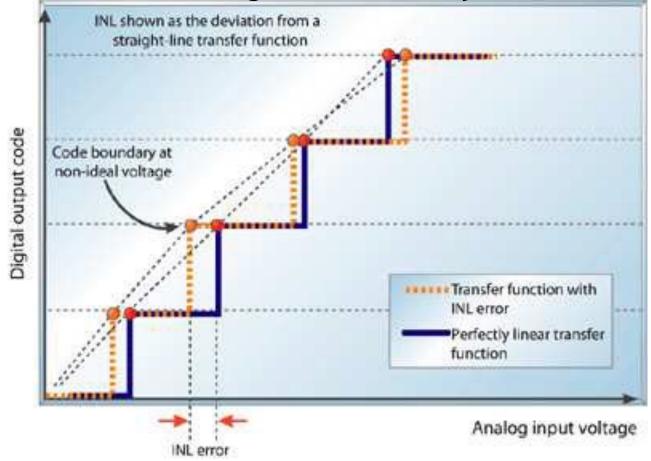
- Figures and some text from:
 - Understanding analog to digital converter speciocations. By Len Staller.
 - https:/archive.eetasia.com/www.eetasia.com/ ART_8800367191_499501_NP_0d2e2745.HTM
- Key concept here is that the specification provides *worst case* values.



Built-in ¹/₂ LSB error corrected

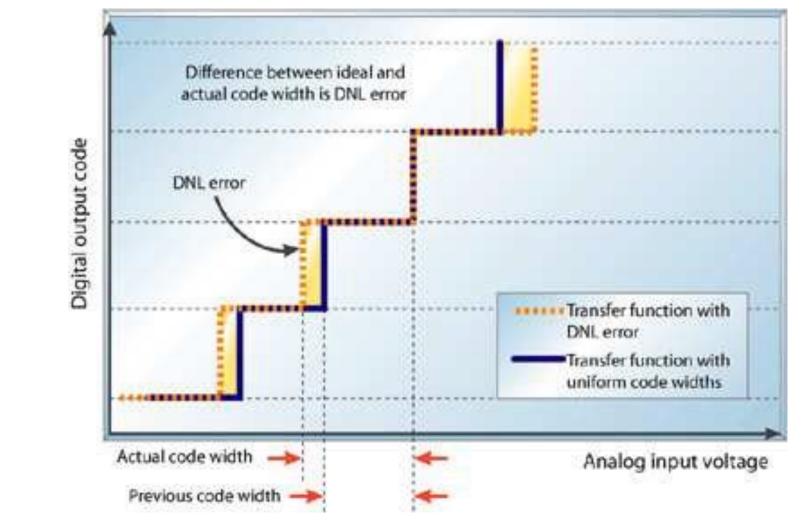


Integral nonlinearity



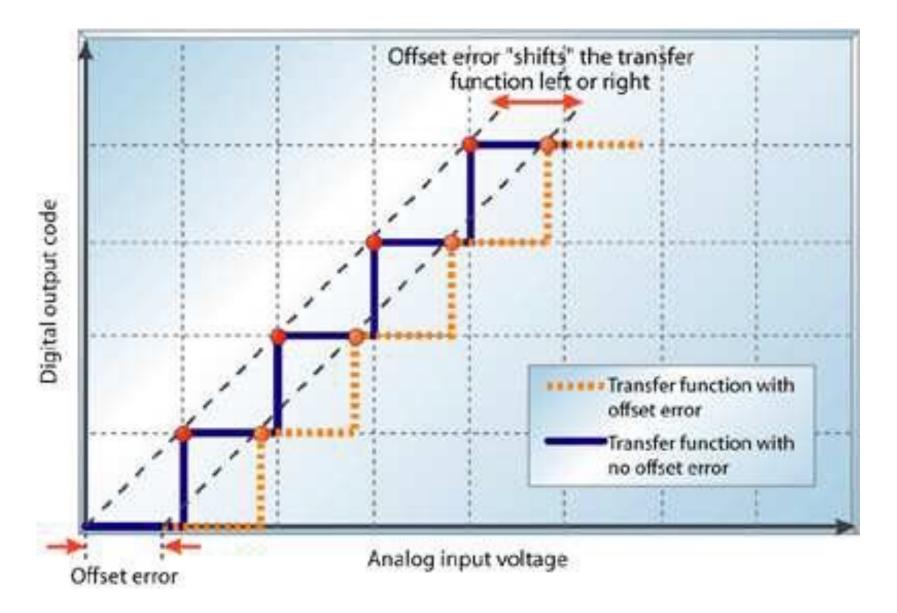
- Deviation of an ADC transfer function from a straight line.
- Best-ot line or highest to lowest points.
- Worst-case voltage deviation over all transitions.
- Express in LSB.
- INL error at any point in transfer function is integral of all lower DNL errors (next page).

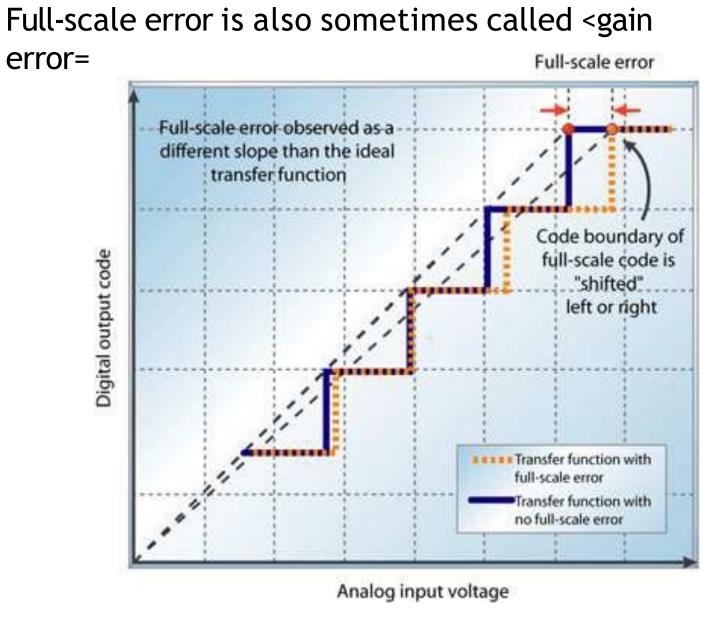
Differential nonlinearity



Worst-cases deviation of step size from ideal.

Offset error





Difference between ideal and actual transition to highest code when offset error is zero.

Errors

• Errors in a specification are bad.

- So if you have an INL of ± 0.25 LSB, you "know" that the device will never have more than 0.25 LSB error.
- Temperature, input voltage, input current, etc.
- Some errors can be compensated for.
 - Nonlinearity.
 - Piece-wise linear lookup table.
 - Device-wise calibration can be expensive.
 - Automated or manufacturing process?
 - What about drift?

Acknowledgements

These slides contain materials from Prabal Dutta, Mark Brehob and Thomas Schmid (UMich)