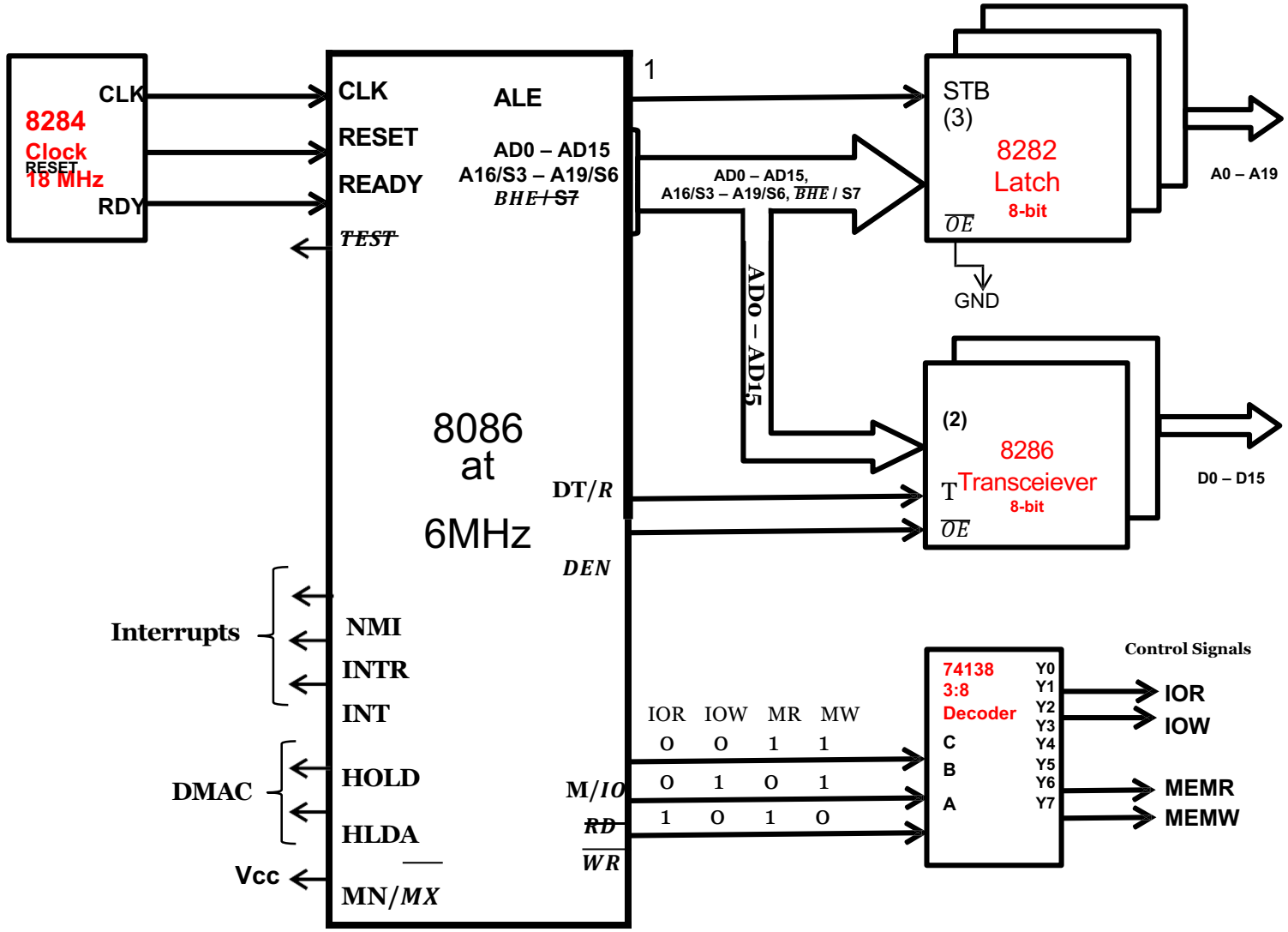
8086 in Maximum Mode

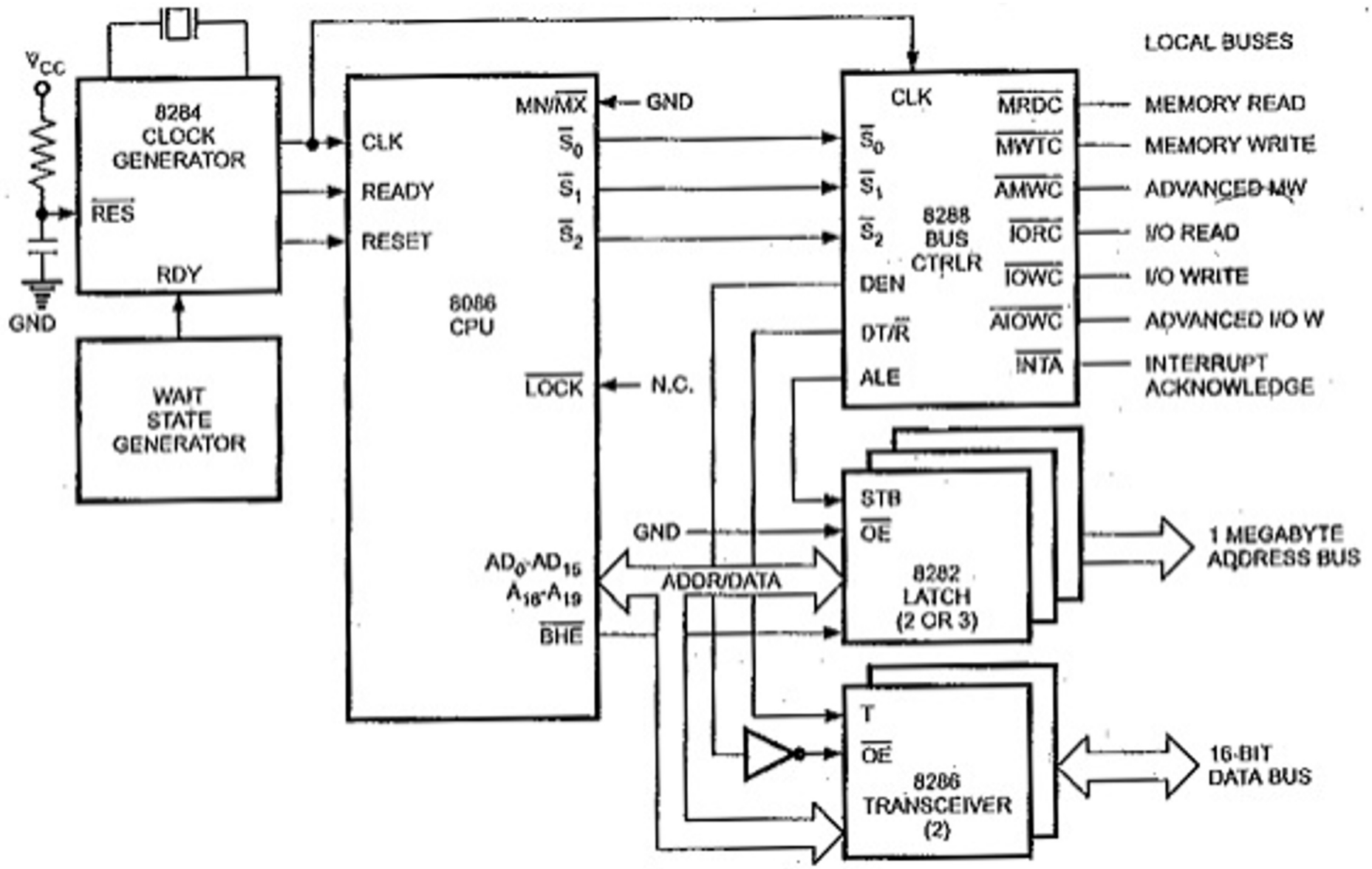
8086 in Minimum Mode!



Maximum Mode Operation

- Differs from minimum mode in that some control signals must be externally generated.
  - requires addition of the 8288 bus controller
- There are not enough pins on the 8086 for bus control during maximum mode
  - new pins and features replaced some of them
- Maximum mode used only when the system contains external coprocessors such as 8087.

Typical Maximum Mode Configuration



The 8288 Bus Controller

- Provides the signals eliminated from the 8086/8088 by the maximum mode operation.

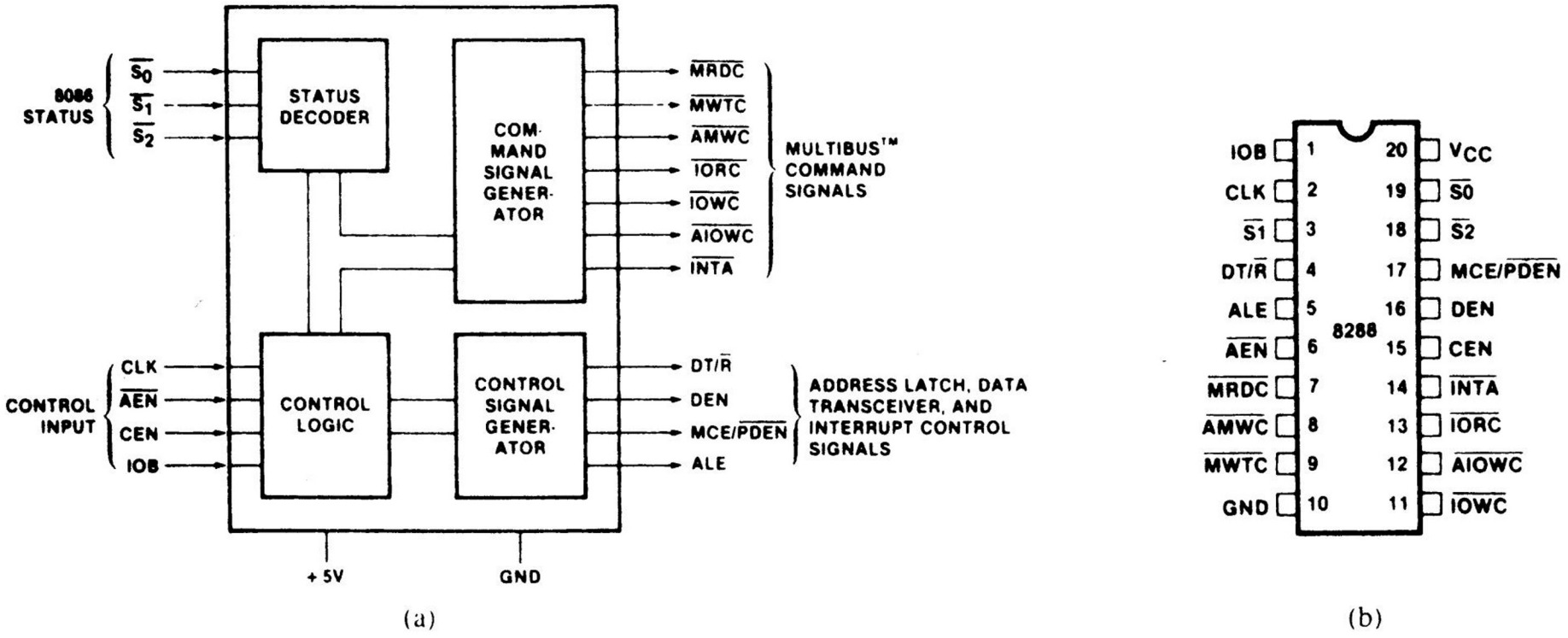
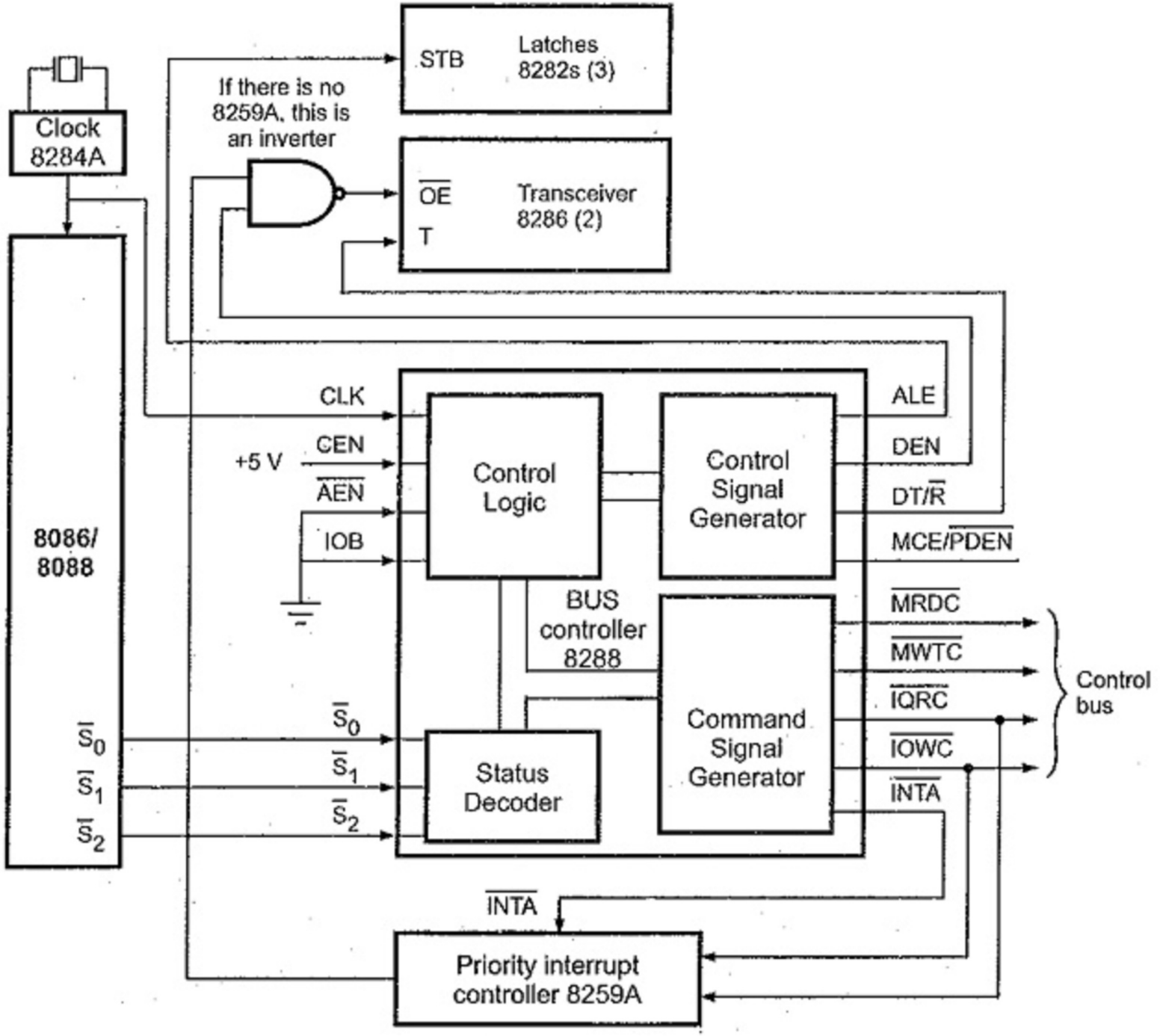


Figure 1. The 8288 bus controller; (a) block diagram and (b) pin-out.

8288 Internal Architecture



8288 Bus Controller *Pin Functions*
S2, S1, and S0

- **Status inputs** are connected to the status output pins on 8086
  - three signals decoded to generate timing signals

$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$	Machine cycle
0	0	0	Interrupt Acknowledge
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt

$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$	Machine cycle
1	0	0	Instruction fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Inactive-Passive

CLK

- The **clock** input provides internal timing.
  - must be connected to the CLK output pin of the 8284A clock generator

8288 Bus Controller *Pin Functions*

ALE

- The **address latch enable** output is used to demultiplex the address/data bus.

DEN

- The **data bus enable** pin controls the bidirectional data bus buffers in the system.

DT/$\overline{R}$

- **Data transmit/receive** signal output to control direction of the bidirectional data bus buffers.

8288 Bus Controller *Pin Functions*

$\overline{\text{AEN}}$

- The **address enable** input causes the 8288 to enable the memory control signals.

CEN

- The **control enable** input enables the command output pins on the 8288.

IOB

- The **I/O bus mode** input selects either I/O bus mode or system bus mode operation.

8288 Bus Controller *Pin Functions*

$\overline{\text{AIOWC}}$

- **Advanced I/O write** is a command output to an advanced I/O write control signal.

$\overline{\text{IORC}}$

- The **I/O read command** output provides I/O with its read control signal.

$\overline{\text{IOWC}}$

- The **I/O write command** output provides I/O with its main write signal.

8288 *Pin Functions*

$\overline{\text{AMWT}}$

- **Advanced memory write** control pin provides memory with an early/advanced write signal.

$\overline{\text{MWTC}}$

- The **memory write** control pin provides memory with its normal write control signal.

$\overline{\text{MRDC}}$

- The **memory read** control pin provides memory with a read control signal.

8288 Bus Controller *Pin Functions*

$\overline{\text{INTA}}$

- The **interrupt acknowledge** output acknowledges an interrupt request input applied to the INTR pin.

MCE/$\overline{\text{PDEN}}$

- The **master cascade/peripheral data** output selects cascade operation for an interrupt controller if IOB is grounded, and enables the I/O bus transceivers if IOB is tied high.

Bus Timings for Maximum Mode Configuration of 8086

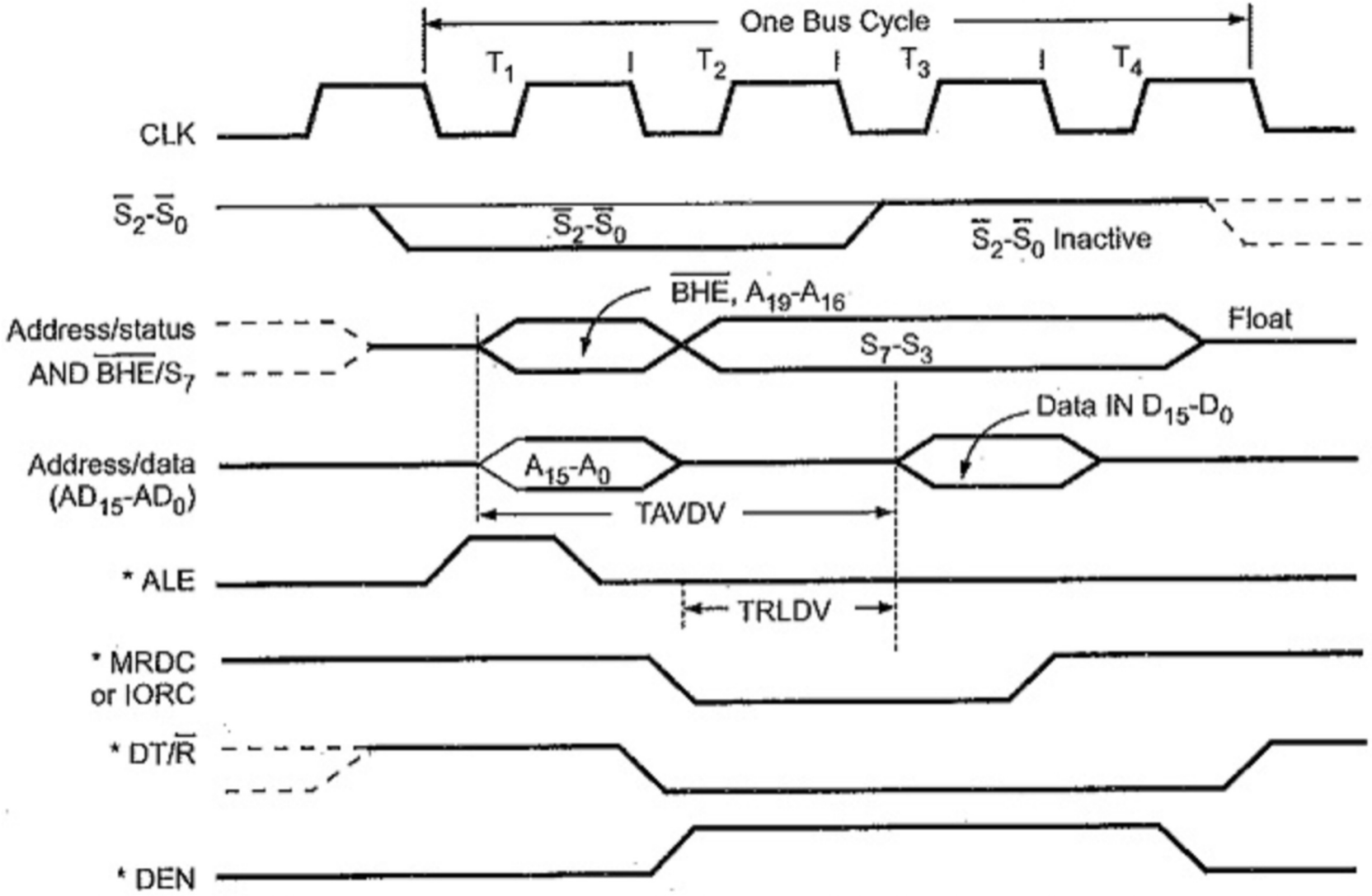
1. S_0,S_1,S_2 are set at the beginning of bus cycle. On detecting the change on passive state $S_0 = S_1 = S_2 = 1$, the 8288 bus controller will output a pulse on its ALE and apply a required signal to its DT/R pin during T_1.

2. In T_2, 8288 will set DEN = 1 thus enabling transceiver. For an input, 8288 it will activate MRDC or IORC. These signals are activated until T_4. For an output, the AMWC or AIOWC is activated from T_2 to T_4 and MWTC or IOWC is activated from T_3 to T_4.

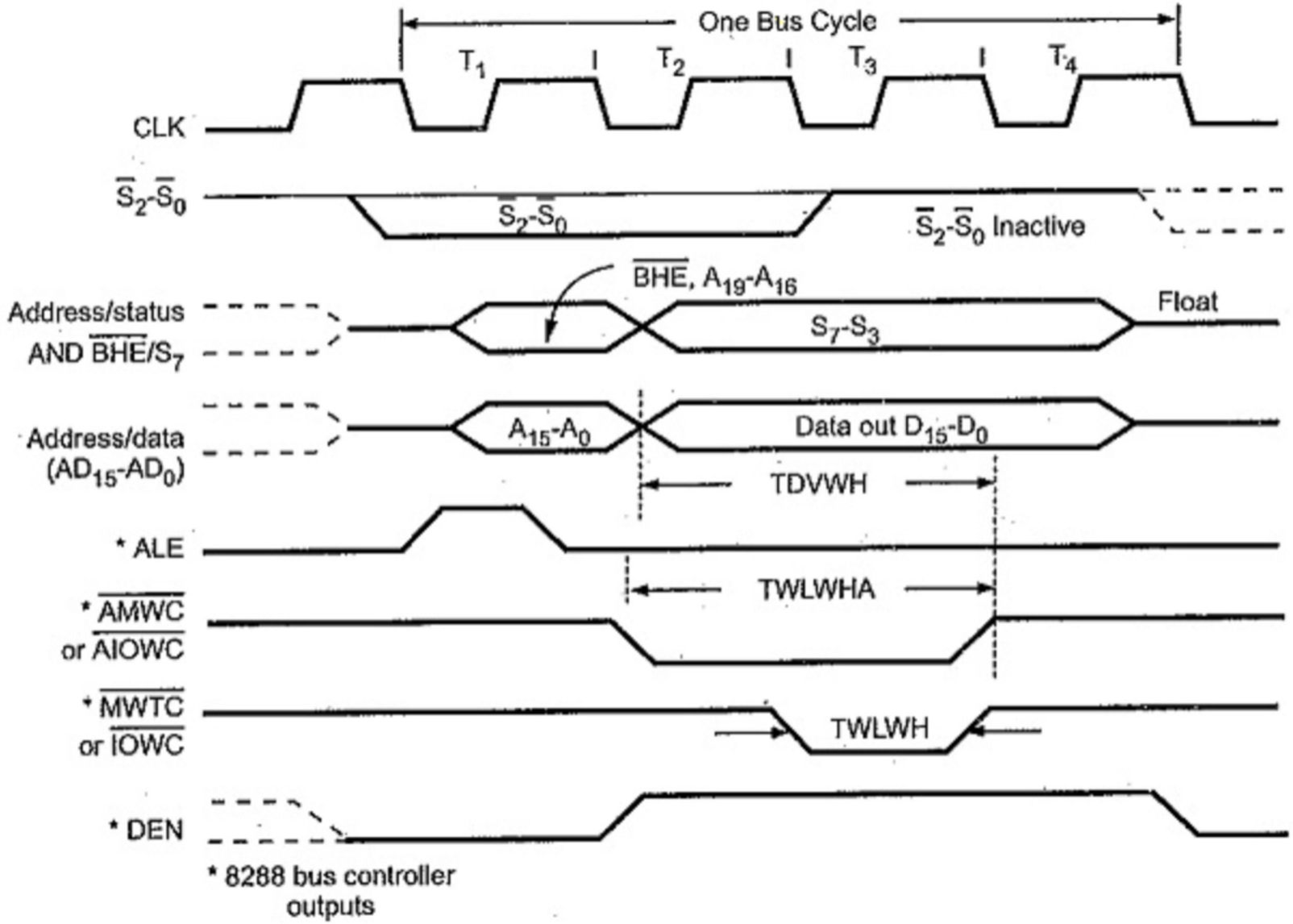
3. The status bits S_0 to S_2 remain active until T_3 and become passive during T_3 and T_4.

4. If READY input is not activated before T3, wait state will be inserted between T_3 and T_4.

Maximum Mode Read



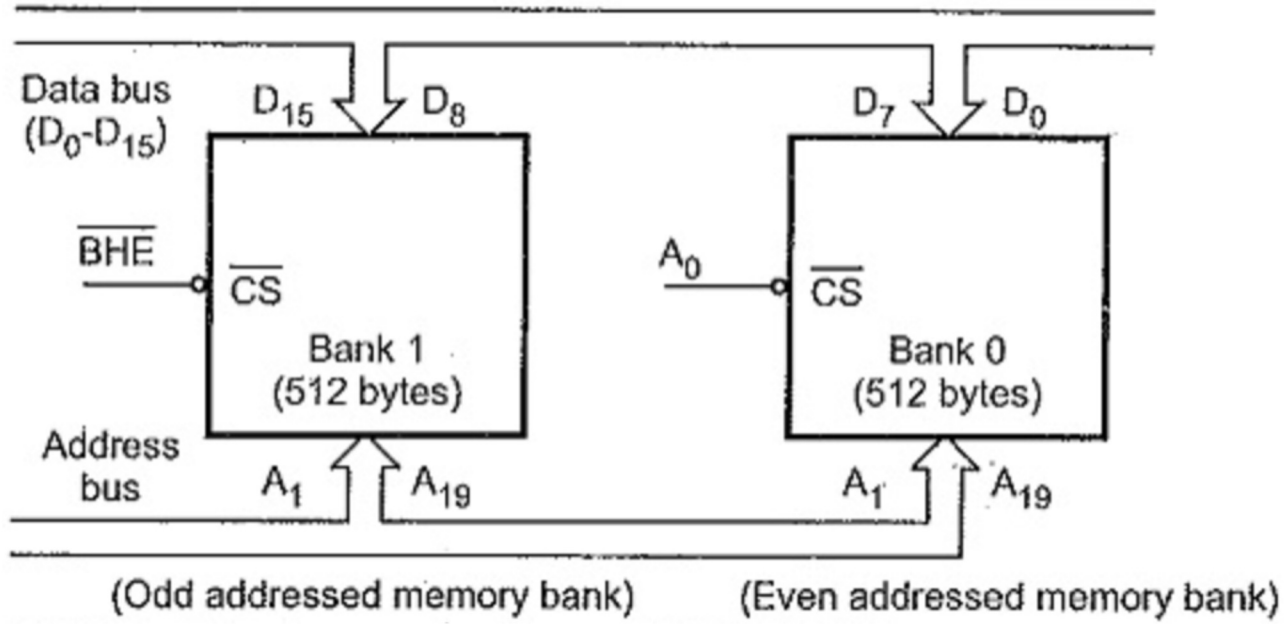
Maximum Mode Write



Memory Addressing Modes of 8086

- Most of the memory ICs are byte oriented
- The 8086 is a 16-bit microprocessor
- In addition to byte, word (16-bit) has to be stored in the memory
- To implement this, the entire memory is divided into two memory banks : $bank_0$ and bank1.
- $Bank_0$ is selected only when A_0 is zero and $Bank_1$ is selected only when BHE is zero.
- A_0 is zero for all even addresses, so $Bank_0$ is usually referred as **even addressed memory** bank. BHE is used to access higher order memory bank, referred to as **odd addressed memory** bank.

No.	Operation	$\overline{BHE}$	A_0	Data Lines Used
1.	Read/Write a byte at an even address	1	0	D_7 - D_0
2.	Read/Write a byte at an odd address	0	1	D_{15} - D_8
3.	Read/Write a word at an even address	0	0	D_{15} - D_0
4.	Read/Write a word at an odd address	0	1	D_{15}-D_0 in first operation byte from odd bank is transferred.
		1	0	D_7-D_0 in second operation byte from even bank is transferred.



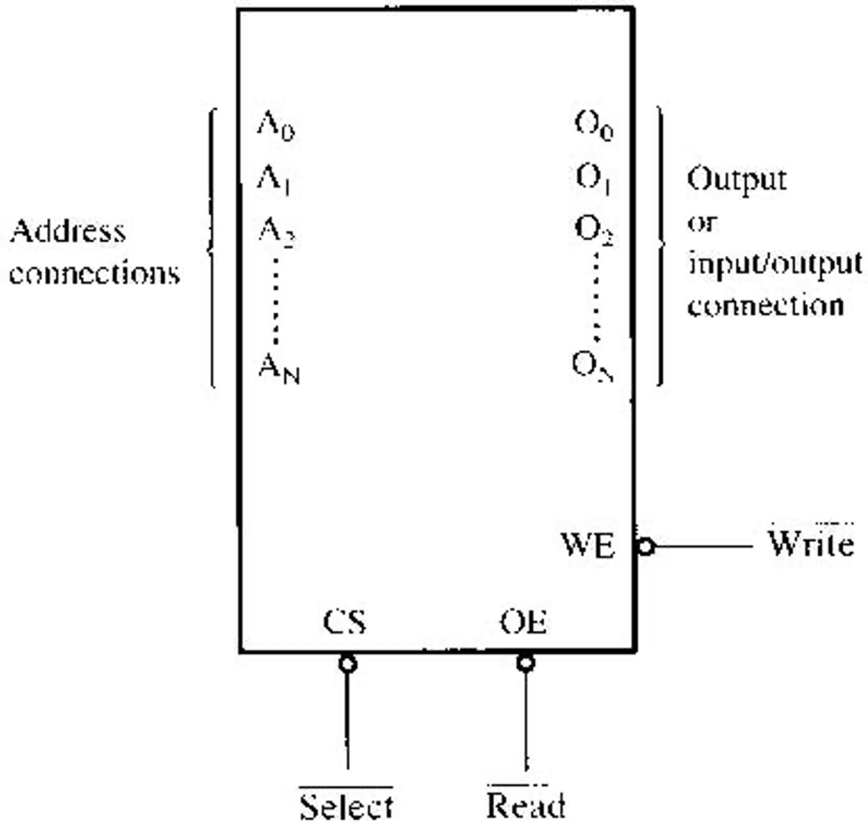
Memory system interfacing

- Every microprocessor-based system has a memory system
- Read-Only Memory (ROM) and Random Access Memory (RAM)
- ROMs / PROMs / EPROMs are mapped to cover the CPU's reset address, since these are non-volatile
- When the 8086 is reset; the next instruction is fetched from memory location FFFF0H. So in the 8086 systems, the location FFFF0H must be ROM location.
- It is important in any memory interface that one block of memory must not be allowed to overlap another memory block.
- In order to connect a memory device to the microprocessor, it is necessary to decode the address from the microprocessor to access each memory IC independently.

MEMORY DEVICES

- Before attempting to interface memory to the microprocessor, it is essential to understand the operation of memory components.
- In this section, we explain functions of the four common types of memory:
  - Read-Only Memory (ROM)
  - Flash memory (EEPROM)
  - Static Random Access Memory (SRAM)
  - Dynamic Random Access Memory (DRAM)

Memory Pin Connections



- address inputs
- data outputs or input/outputs
- some type of selection input
- at least one control input to select a read or write operation

A pseudomemory component illustrating the address, data, and control connections.

Address Connections

- Memory devices have address inputs to select a memory location within the device.
- Almost always labeled from A_0, the least significant address input, to A_n
  - where subscript n can be any value
  - always labeled as one less than total number of address pins
- A memory device with 10 address pins has its address pins labeled from A_0 to A_9.

- The number of address pins on a memory device is determined by the number of memory locations found within it.
- Today, common memory devices have between 1K (1024) to 1G (1,073,741,824) memory locations.
  - with 4G and larger devices on the horizon
- A 1K memory device has 10 address pins.
  - therefore, 10 address inputs are required to select any of its 1024 memory locations

- It takes a 10-bit binary number to select any single location on a 1024-location device.
  - 1024 different combinations
  - if a device has 11 address connections, it has 2048 (2K) internal memory locations
- The number of memory locations can be extrapolated from the number of pins.

Data Connections

- All memory devices have a set of data outputs or input/outputs.
  - today, many devices have bidirectional common I/O pins
  - data connections are points at which data are entered for storage or extracted for reading
- Data pins on memory devices are labeled D_0 through D_7 for an 8-bit-wide memory device.

- An 8-bit-wide memory device is often called a **byte-wide** memory.
  - most devices are currently 8 bits wide,
  - some are 16 bits, 4 bits, or just 1 bit wide
- Catalog listings of memory devices often refer to memory locations times bits per location.
  - a memory device with 1K memory locations and 8 bits in each location is often listed as a 1K × 8 by the manufacturer
- Memory devices are often classified according to total bit capacity.

Selection Connections

- Each memory device has an input that selects or enables the memory device.
  - sometimes more than one
- This type of input is most often called a **chip select** ($\overline{CS}$) **chip enable** ($\overline{CE}$) or simply **select** ($\overline{S}$) input.
- RAM memory generally has at least one or input, and ROM has at least one
- If more than one $\overline{CE}$ connection is present, all must be activated to read or write data.

Control Connections

All memory devices have some form of control input or inputs.

ROM usually has one control input, while RAM often has one or two control inputs

- Control input often found on ROM is the **output enable** or **gate** connection, which allows data flow from output data pins.
- The $\overline{OE}$ connection enables and disables a set of three-state buffers located in the device and must be active to read data.

- RAM has either one or two control inputs.
  - if one control input, it is often called R/$\overline{W}$
- If the RAM has two control inputs, they are usually labeled $\overline{WE}$ (or $\overline{W}$), and $\overline{OE}$ (or $\overline{G}$).
  - **write enable** must be active to perform memory write, and OE active to perform a memory read
  - when the two controls are present, they must never both be active at the same time
- If both inputs are inactive, data are neither written nor read.
  - the connections are at their high-impedance state

ROM Memory

- **Read-only memory** (ROM) permanently stores programs/data resident to the system.
  - and must not change when power disconnected
- Often called **nonvolatile memory**, because its contents *do not* change even if power is disconnected.
- A device we call a ROM is purchased in mass quantities from a manufacturer.
  - programmed during fabrication at the factory

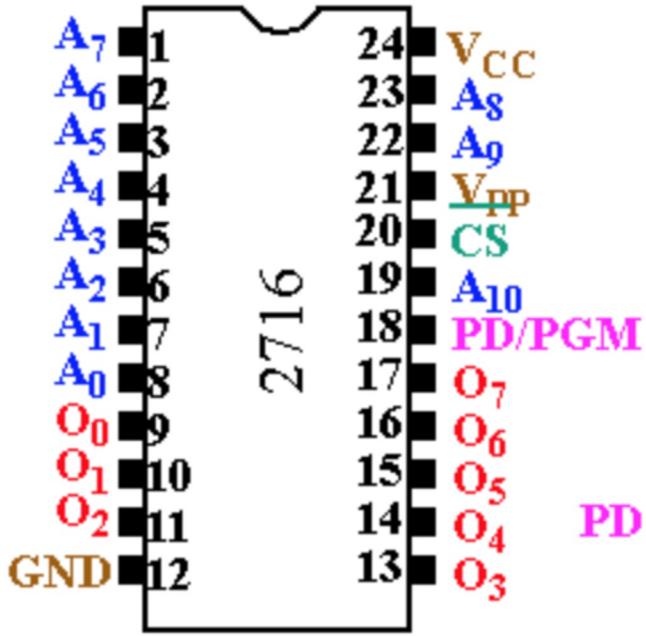
- The EPROM (**erasable programmable read-only memory**) is commonly used when software must be changed often.
  - or when low demand makes ROM uneconomical
  - for ROM to be practical at least 10,000 devices must be sold to recoup factory charges
- An EPROM is programmed in the field on a device called an EPROM programmer.
- Also erasable if exposed to high-intensity ultraviolet light.
  - depending on the type of EPROM

- PROM memory devices are also available, although they are not as common today.
- The PROM (**programmable read-only memory**) is also programmed in the field by burning open tiny NI-chrome or silicon oxide fuses.
- Once it is programmed, it cannot be erased.

- A newer type of **read-mostly memory** (RMM) is called the **flash memory**.
  - also often called an EEPROM (**electrically erasable programmable ROM**)
  - EAROM (**electrically alterable ROM**)
  - or a NOVRAM (**nonvolatile RAM**)
- Electrically erasable in the system, but they require more time to erase than normal RAM.
- The flash memory device is used to store setup information for systems such as the video card in the computer.

- Flash has all but replaced the EPROM in most computer systems for the BIOS.
  - some systems contain a password stored in the flash memory device
- Flash memory has its biggest impact in memory cards for digital cameras and memory in MP3 audio players.
- Figure 2 illustrates the 2716 EPROM, which is representative of most common EPROMs.

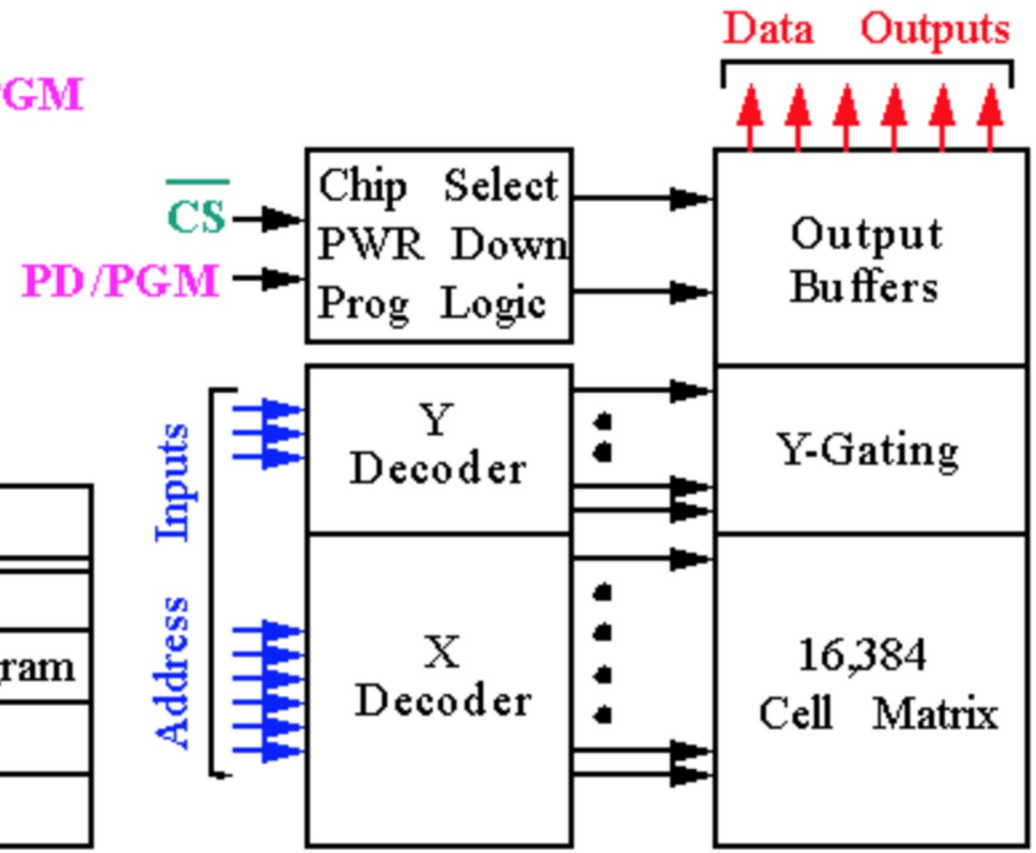
Figure 2 The pin-out of the 2716, 2K × 8 EPROM



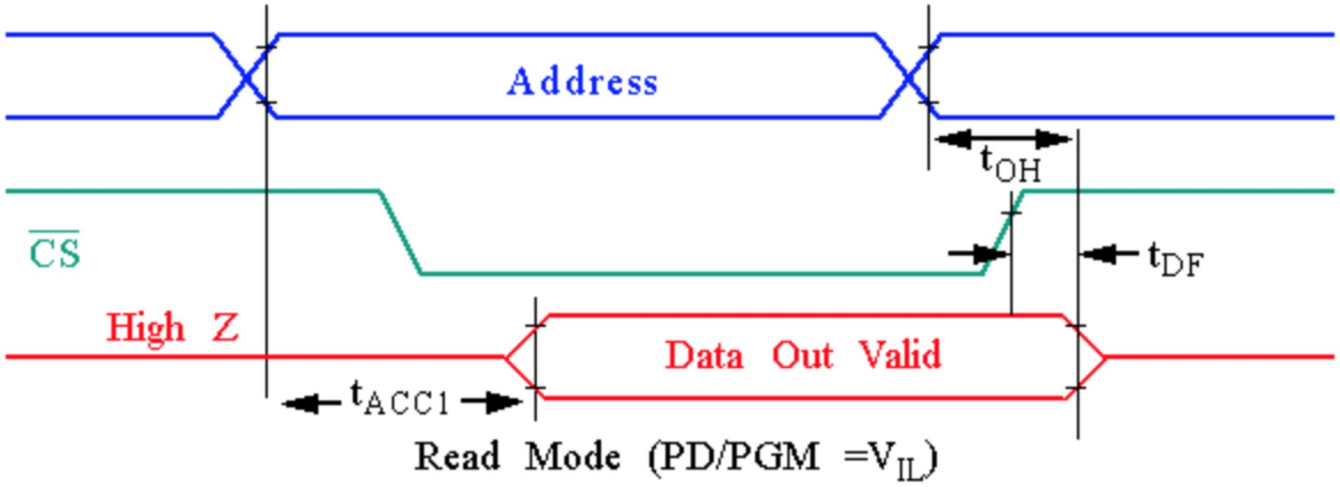
2K x 8 EPROM

Pin(s)	Function
A_0-A_{10}	Address
PD/PGM	Power down/Program
$\overline{CS}$	Chip Select
O_0-O_7	Outputs

V_{PP} is used to program the device by applying 25V and pulsing PGM while holding $\overline{CS}$ high.



2716 Timing Diagram



- *Sample of the data sheet for the 2716 A.C. Characteristics.*

Symbol	Parameter	Limits			Unit	Test Condition
		Min	Typ.	Max		
tACC1	Addr. to Output Delay		250	450	ns	PD/PGM= CS =VIL
tOH	Addr. to Output Hold	0			ns	PD/PGM= CS =VIL
tDF	Chip Deselect to Output Float	0		100	ns	PD/PGM=VIL
...	...	...	...	...	...	...

- *This EPROM requires a wait state for use with the 8086 (460ns constraint).*

- Figure 3 illustrates the timing diagram for the 2716 EPROM.
- The V_{PP} pin must be placed at a logic 1 level for data to be read from the EPROM.
- In some cases, the V_{PP} pin is in the same position as the $\overline{WE}$ pin on the SRAM.
- This will allow a single socket to hold either an EPROM or an SRAM.
  - an example is the 27256 EPROM and 62256 SRAM, both 32K × 8 devices with the same pin-out, except for V_{PP} on the EPROM and $\overline{WE}$ on the SRAM.

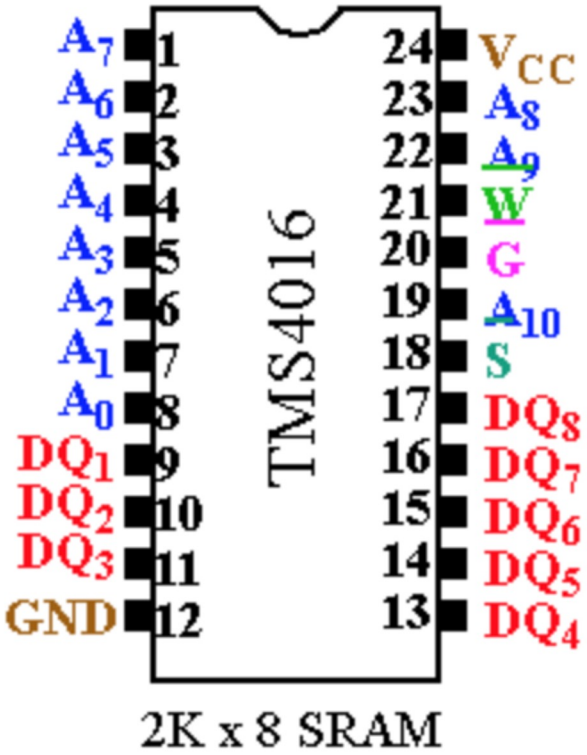
- The basic speed of this EPROM is 450 ns.
  - recall that 8086 operated with a 5 MHz clock allowed memory 460 ns to access data
- This type of component requires wait states to operate properly with 8086 because of its rather long access time.
  - if wait states are not desired, higher-speed EPROMs are available at additional cost
  - EPROM memory is available with access times of as little as 100 ns
- Obviously, wait states are required in modern microprocessors for any EPROM device.

Static RAM (SRAM) Devices

- Static RAM memory devices retain data for as long as DC power is applied.
- Because no special action is required to retain data, these devices are called **static memory**.
  - also called **volatile memory** because they will not retain data without power
- The main difference between ROM and RAM is that RAM is written under normal operation, whereas ROM is programmed outside the computer and normally is only read.

- Fig 4 illustrates the 4016 SRAM,
  - a 2K × 8 read/write memory
- This device is representative of all SRAM devices.
  - except for the number of address and data connections.
- The control inputs of this RAM are slightly different from those presented earlier.
  - however the control pins function exactly the same as those outlined previously
- Found under part numbers 2016 and 6116.

Figure 4 The pin-out of the TMS4016, 2K × 8 static RAM (SRAM). (Courtesy of Texas Instruments Incorporated.)



Pin(s)	Function
A_0-A_{10}	Address
DQ_0-DQ_7	Data In/Data Out
S (CS)	Chip Select
G (OE)	Read Enable
W (WE)	Write Enable

- *Virtually identical to the EPROM with respect to the pinout.*
- *However, access time is faster (250ns).*
  - *See the timing diagrams and data sheets in text.*
- *SRAMs used for caches have access times as low as 10ns .*

- Figure 6 illustrates pin-outs of the 62256, 32K × 8 static RAM.
- Packaged in a 28-pin integrated circuit
- Available with access times of 120 or 150 ns.
- Other common SRAM devices are
  - 8K × 8; 128K × 8; 256K × 8
  - 512K × 8; 1M × 8
- Access times can be as low as 1.0 ns for SRAM used in computer cache memory.

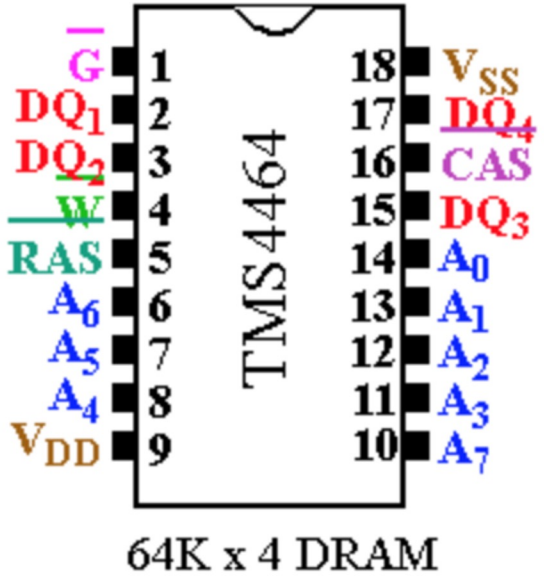
Dynamic RAM (DRAM) Memory

- Available up to 256M × 8 (2G bits).
- DRAM is essentially the same as SRAM, except that it retains data for only 2 or 4 ms on an integrated capacitor.
- After 2 or 4 ms, the contents of the DRAM must be completely rewritten *(refreshed)*.
  - because the capacitors, which store a logic 1 or logic 0, lose their charges

- In DRAM, the entire contents are refreshed with 256 reads in a 2- or 4-ms interval.
  - also occurs during a write, a read, or during a special refresh cycle
- DRAM requires so many address pins that manufacturers multiplexed address inputs.
- Figure 7 illustrates a 64K × 4 DRAM, the TMS4464, which stores 256K bits of data.
  - note it contains only eight address inputs where it should contain 16—the number required to address 64K memory locations

Figure 7 The pin-out of the TMS4464, 64K × 4 dynamic RAM (DRAM). (Courtesy of Texas Instruments Incorporated.)

- *TI TMS4464 DRAM (64K X 4):*



64K x 4 DRAM

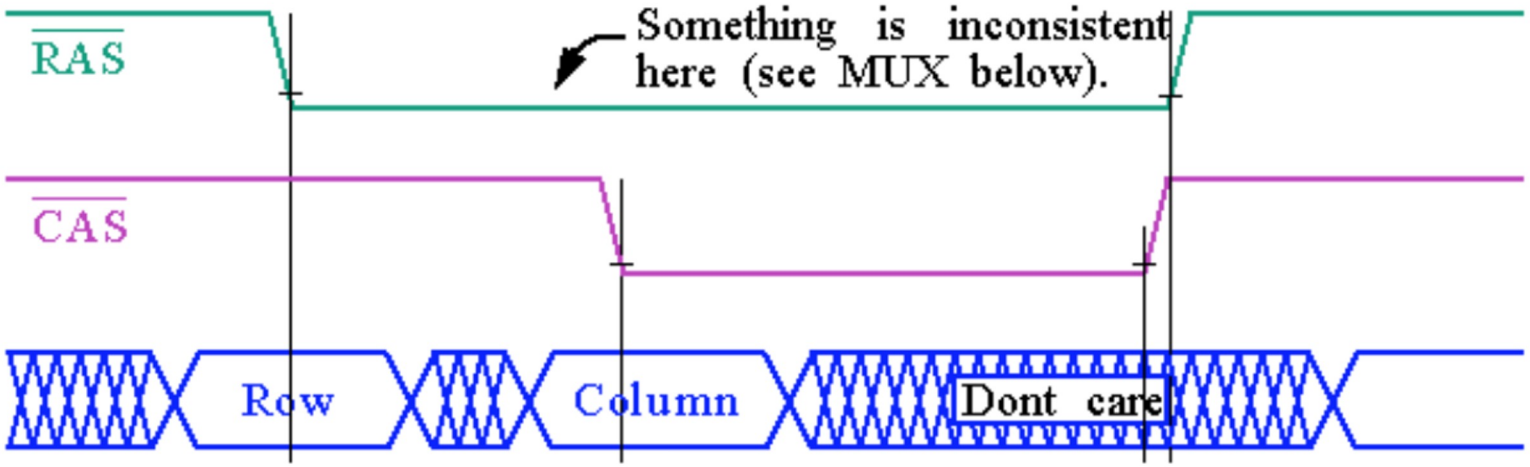
Pin(s)	Function
A_0-A_7	Address
DQ_0-DQ_4	Data In/Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable

  - *The TMS4464 can store a total of 256K bits of data.*

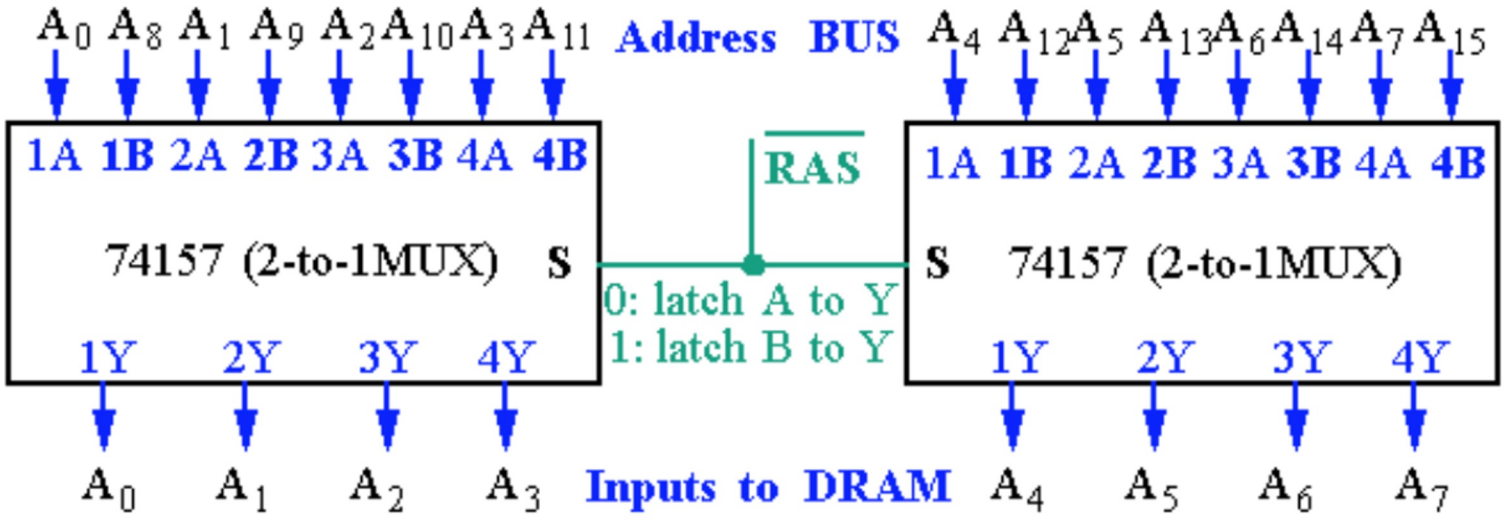
- 16 address bits can be forced into eight address pins in two 8-bit increments
- this requires two special pins: the **column address strobe** ($\overline{CAS}$) and **row address strobe** ($\overline{RAS}$)

- First, A_0–A_7 are placed on the address pins and strobed into an internal row latch by $\overline{RAS}$ as the row address.
- Next, address bits A_8-A_{15} are placed on the same eight address inputs and strobed into an internal column latch by $\overline{CAS}$ as the column address
- The 16-bit address in the internal latches addresses the contents of one of the 4-bit memory locations.
  - $\overline{CAS}$ also performs chip selection input to DRAM

Figure 8 $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and address input timing for the TMS4464 DRAM. (Courtesy of Texas Instruments Incorporated.)

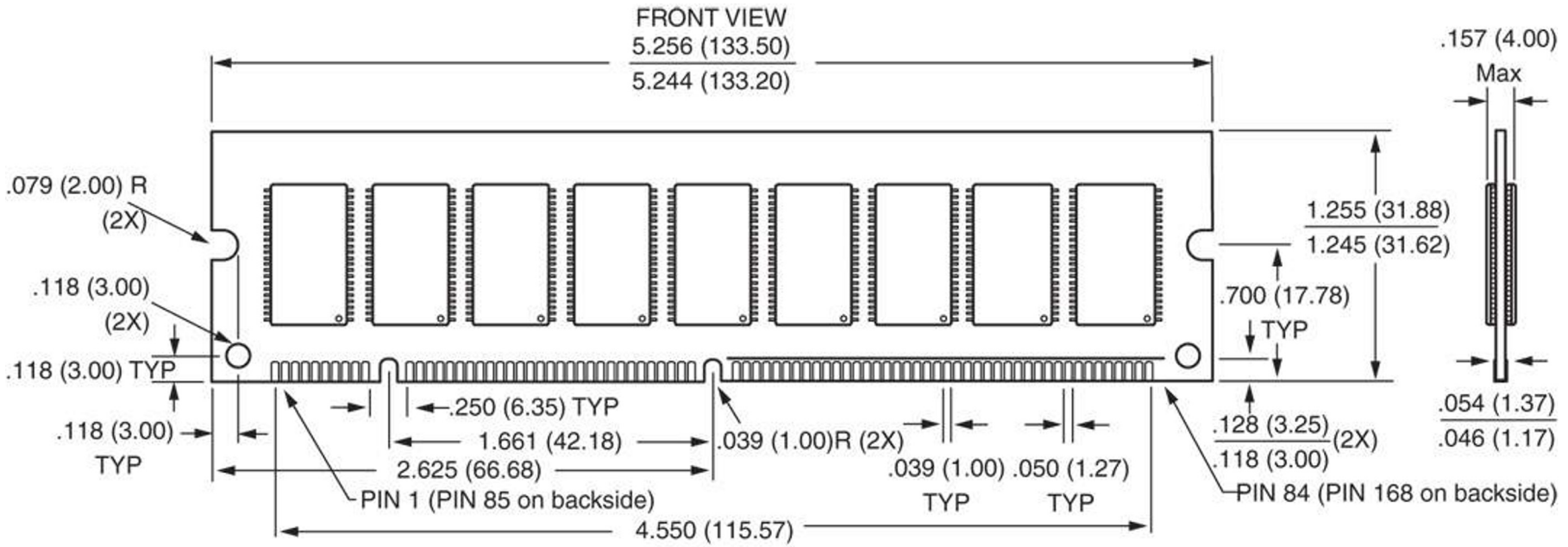


- CAS *also performs the function of the chip select input.*



- multiplexers used to strobe column and row addresses into the address pins on a pair of TMS4464 DRAMs.
- the RAS signal not only strobes the row address into the DRAMs, but it also selects which part of the address is applied to the address inputs.

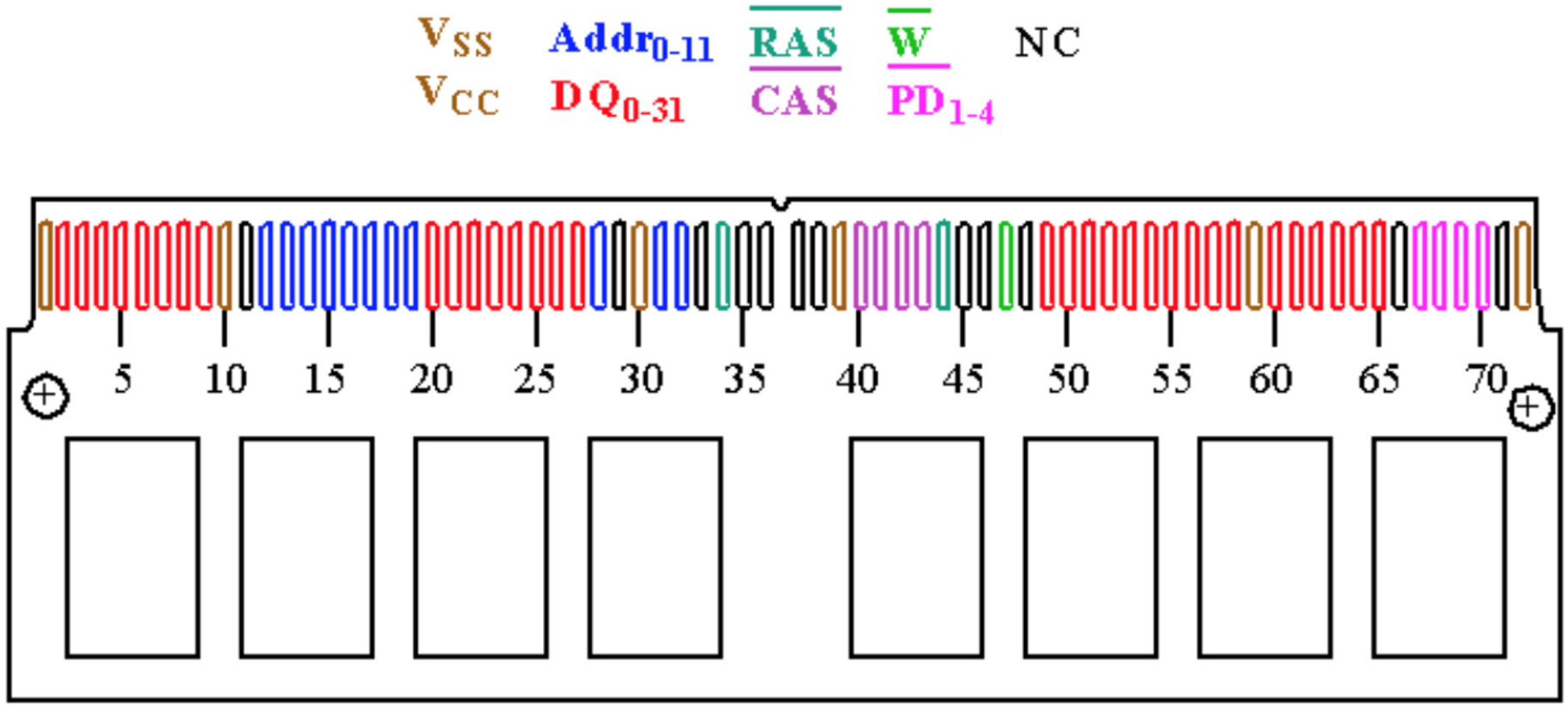
Figure 10 The 41256 dynamic RAM organized as a 256K × 1 memory device.



- the pin-out of the 41256 dynamic RAM
- this device is organized as a 256K × 1 memory
- requires as little as 70 ns to access data

- DRAM is often placed on small boards called SIMMs (Single In-Line Memory Modules).
- The 30-pin SIMM is organized most often as 1M × 8 or 1M × 9, and 4M × 8 or 4M × 9.
  - illustrated in Fig 11 is a 4M × 9
  - the ninth bit is the parity bit
- Also shown is a newer 72 pin SIMM.
- 72-pin SIMMs are often organized as 1M × 32 or 1M × 36 (with parity).
- Fig 11 illustrates a 4M × 36 SIMM, which has 16M bytes of memory

Figure 10–11 The pin-outs of the 30-pin and 72-pin SIMM. 72-pin SIMM organized as 4M × 32.



- Pentium–Pentium 4 microprocessors have a 64-bit wide data bus, which precludes use of the 8-bit-wide SIMMs described here.
  - 72-pin SIMMs are cumbersome as they must be paired to obtain a 64-bit-wide data connection
- 64-bit-wide DIMMs (Dual In-line Memory Modules) have become the standard.
- The memory on these modules is organized as 64 bits wide.
- Common sizes available are from 16M bytes (2M × 64) to 1G bytes (128M × 64).

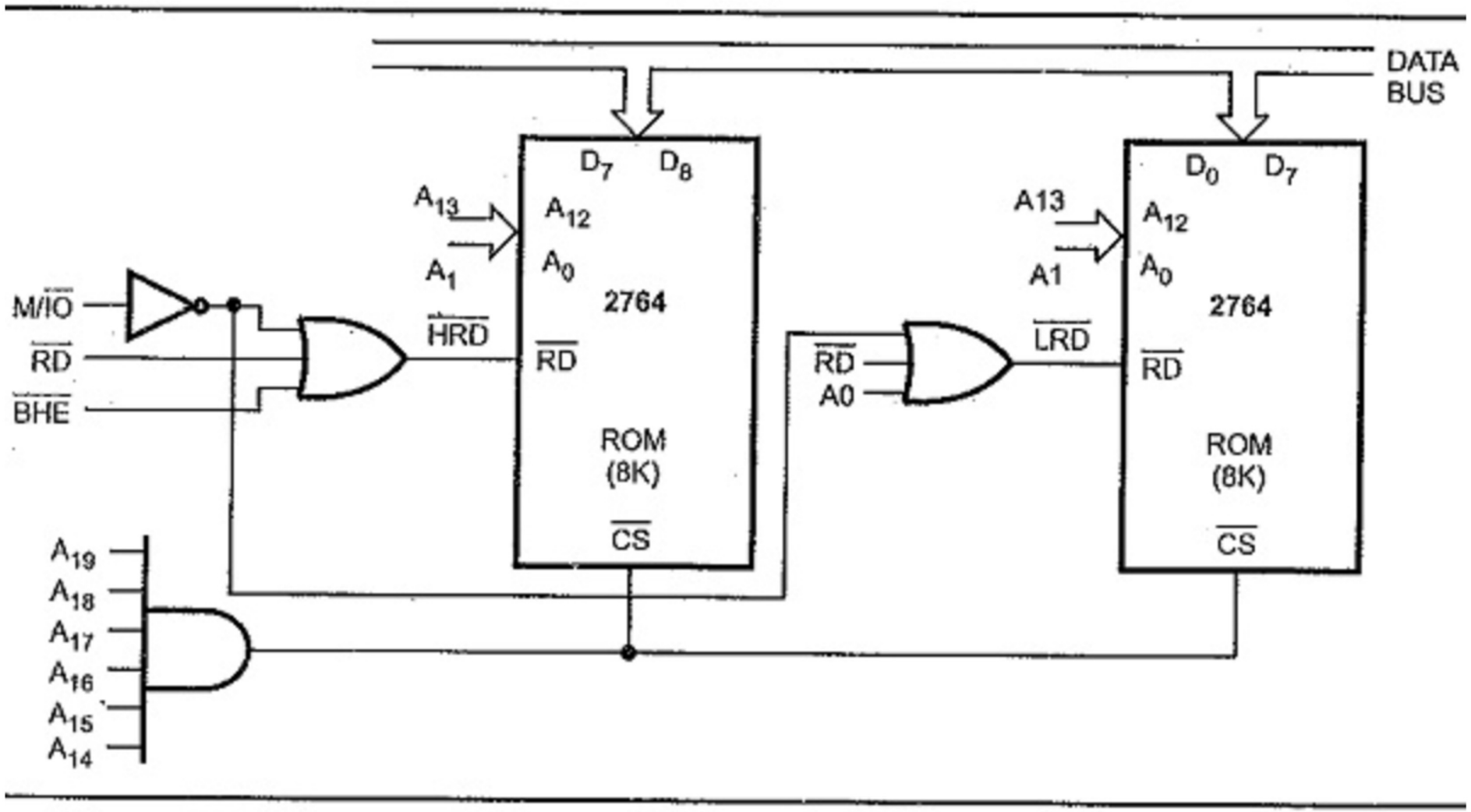
Address decoding techniques in 8086

- Absolute decoding
- Linear decoding
- Block decoding

Absolute decoding

- Memory chip is selected only for the specified logic level on the address lines
- No other logic levels can select the chip.
- Example: two 8K EPROMs (2764) are used to provide even and odd memory banks.
  - Control signals BHE and A_0 are used to enable outputs of odd and even memory banks
  - As each memory chip has 8K memory locations, thirteen address lines are required to address each locations
  - All remaining address lines are used to generate an unique chip select signal.
  - This addressing technique is normally used in large, memory systems.

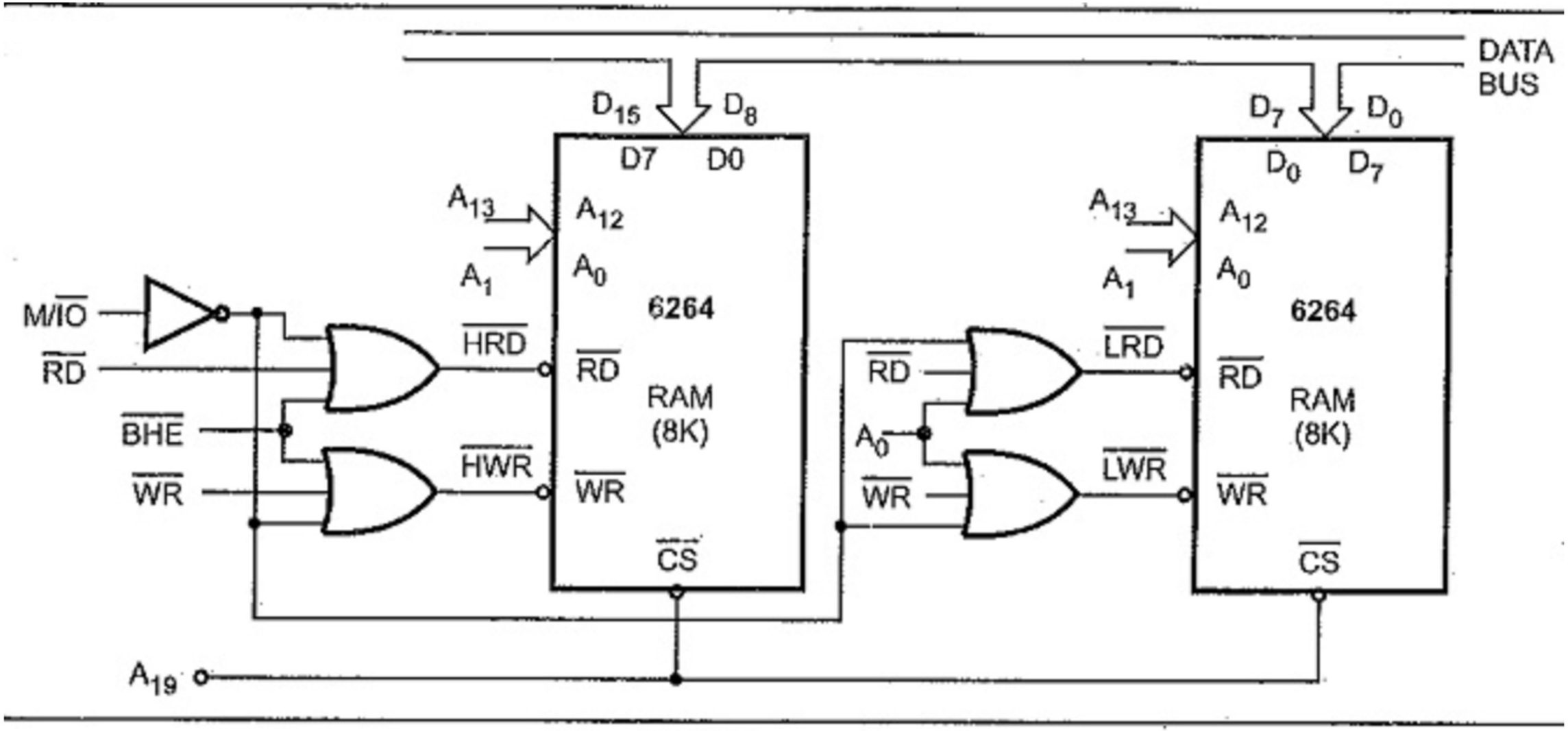
Absolute decoding example



Linear decoding

- In small systems, hardware for the decoding logic can be eliminated by using only required number of addressing lines
- This technique is referred as **Linear Decoding** or **Partial Decoding**
- Example: the addressing of 16K RAM (6264) with linear decoding
  - Control signals BHE and A_0 are used to enable odd and even memory banks, respectively.
  - The address line A_{19} is used to select the RAM chips.
  - When A_{19} is low, chip is selected, otherwise it is disabled.
  - The status of A_{14} to A_{18} does not affect the chip selection logic.
  - This gives you multiple addresses (shadow addresses)

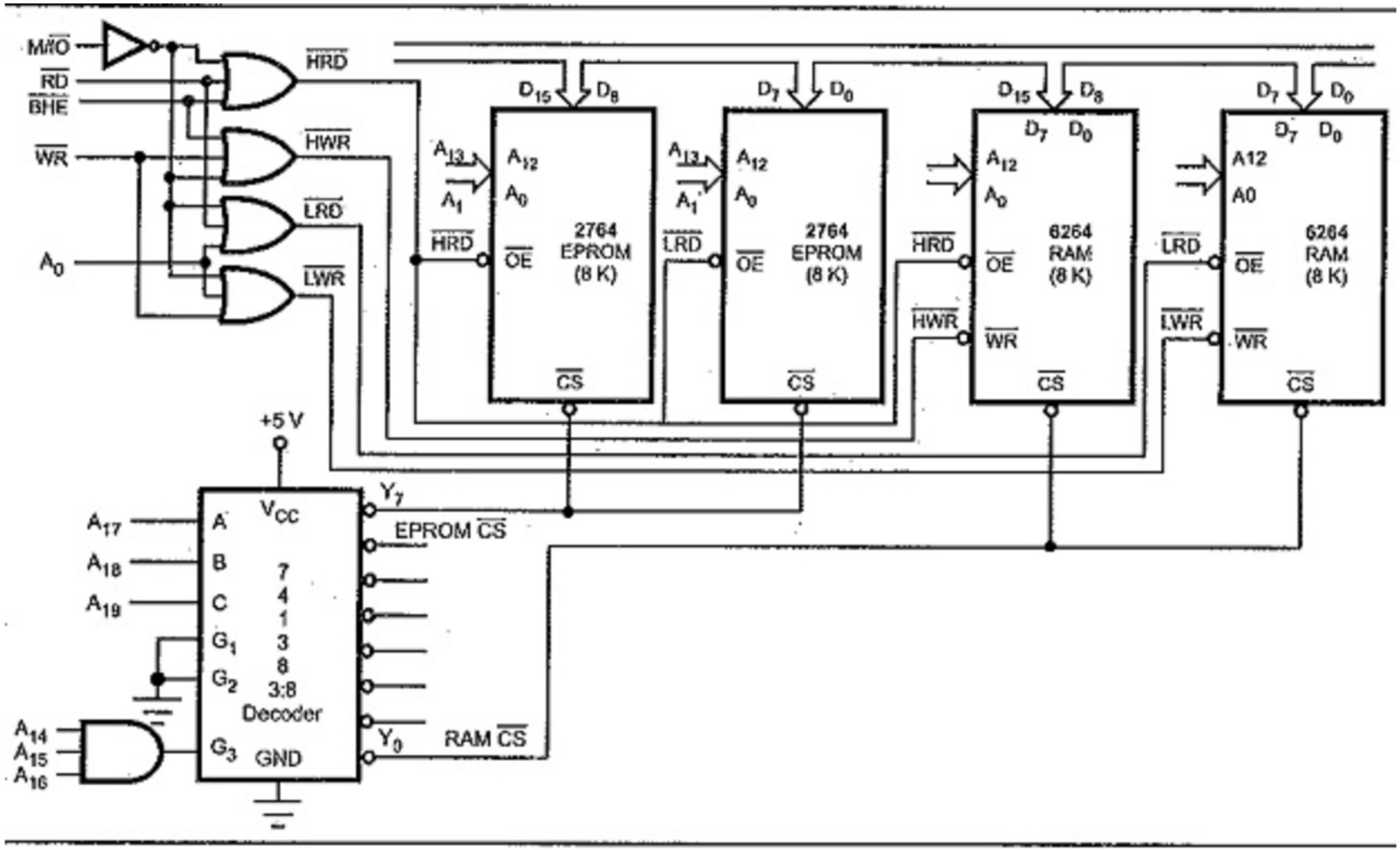
Linear decoding example



Block decoding

- Memory array often consists of several blocks of memory chips.
- Each block of memory requires a decoding circuit.
- To avoid separate decoding for each memory block a special decoder IC is used to generate chip select signal for each block.
- The example shows the block Address Decoding Techniques in 8086 Microprocessor using a 74138, 3:8 decoder.

Block decoding example




That's all Folks!