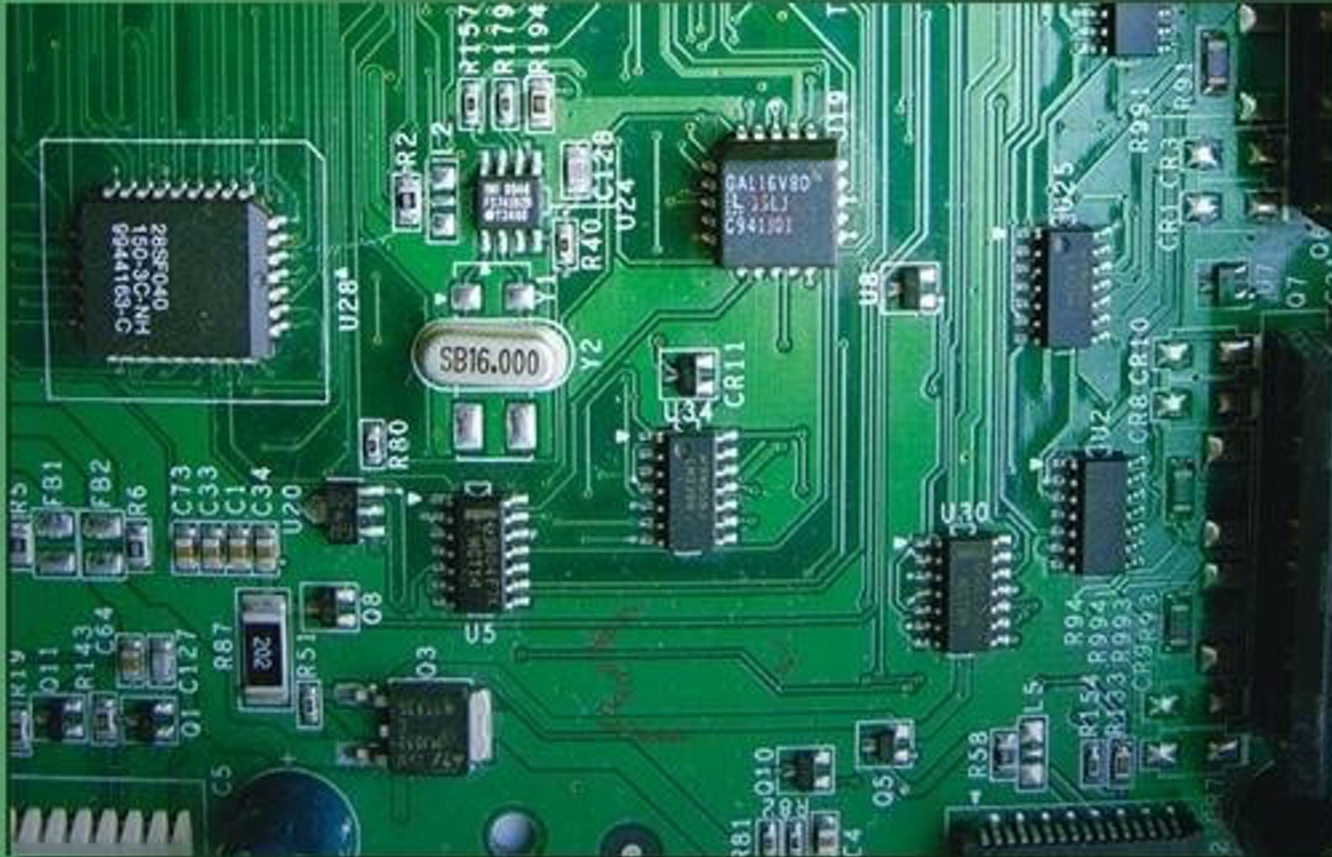


The Intel Microprocessors

8086/8088, 80186/80188, 80286, 80386, 80486 Pentium, Pentium Pro Processor, Pentium II, Pentium 4, and Core2 with 64-bit Extensions

Architecture, Programming, and Interfacing



EIGHTH EDITION

Barry B. Brey

PEARSON

Chapter 9: 8086/8088 Hardware Specifications

Introduction

- In this chapter, the **pin functions** of the 8086 microprocessor are detailed and information is provided on the following hardware topics: **clock generation, bus buffering, bus latching, timing, wait states, and minimum mode operation versus maximum mode operation.**
- These simple microprocessors are explained as an introduction to the Intel microprocessor family.

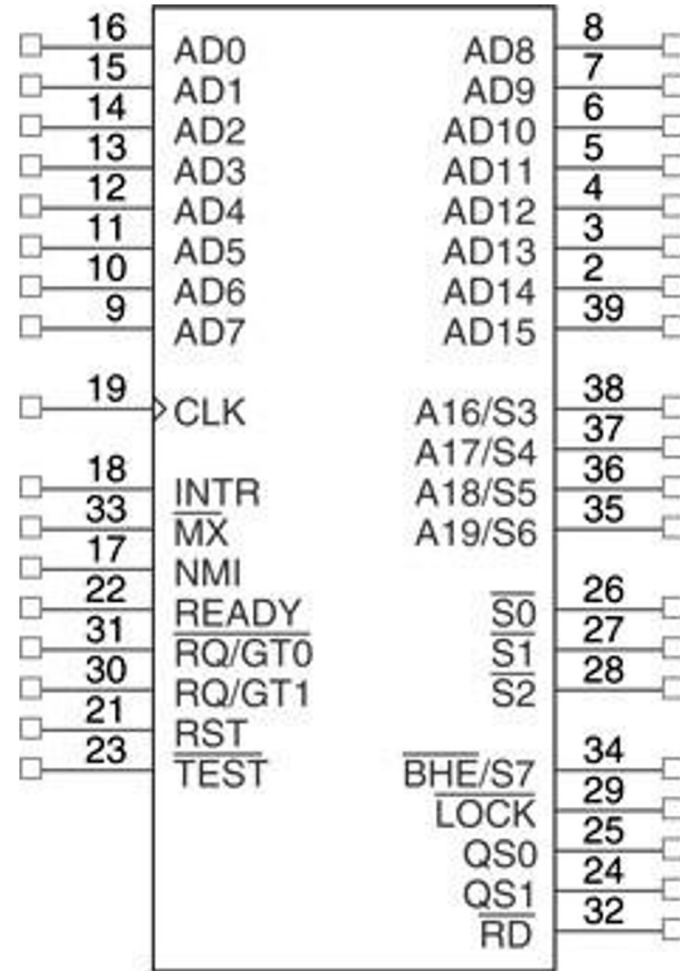
PIN-OUTS AND THE PIN FUNCTIONS

- In this section, we explain the function and the **multiple functions** of each of the microprocessor's pins.
- In addition, we discuss the **DC characteristics** to provide a basis for understanding the later sections on **buffering** and **latching**.

The Pin-Out

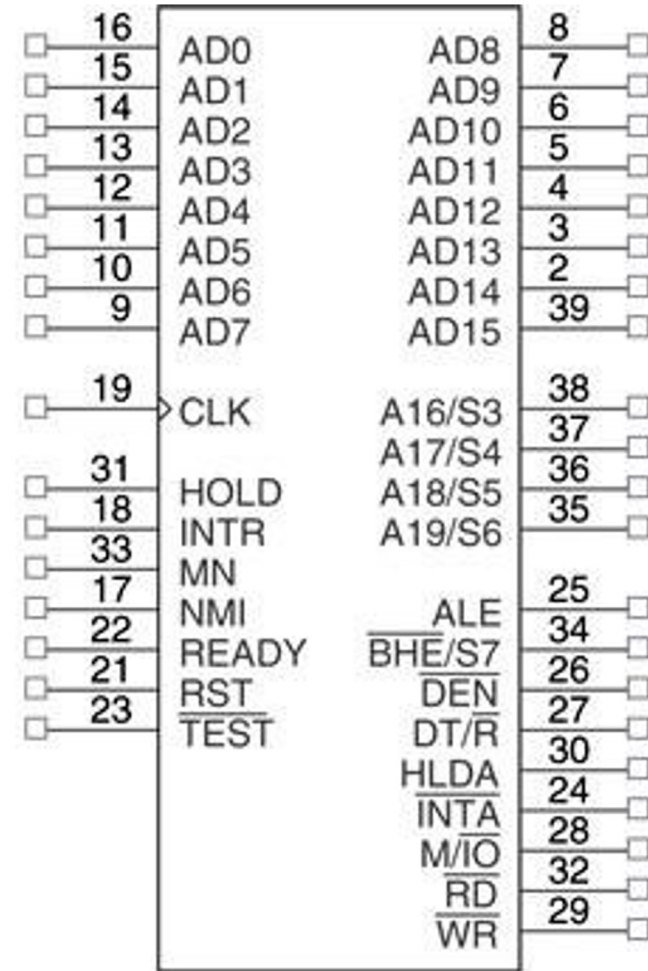
- Figure 1 illustrates pin-outs of 8086.
 - packaged in 40-pin **dual in-line** package (**DIP**)
- 8086 is a **16-bit** microprocessor with a 16-bit data bus;
 - 8086 has pin connections **AD_0-AD_{15}**

Figure 1 (a) The pin-out of the 8086 in **maximum mode**;
 (b) the pin-out of the 8086 in **minimum mode**.



8086MAX

(a)

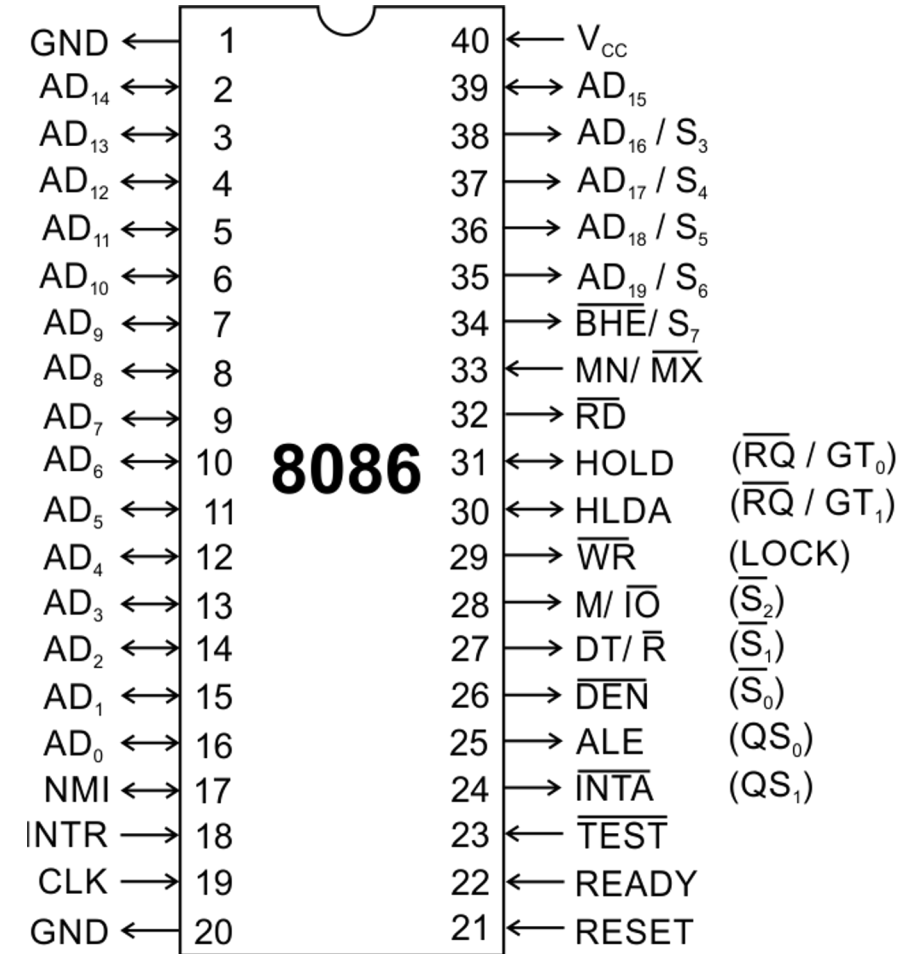


8086MIN

(b)

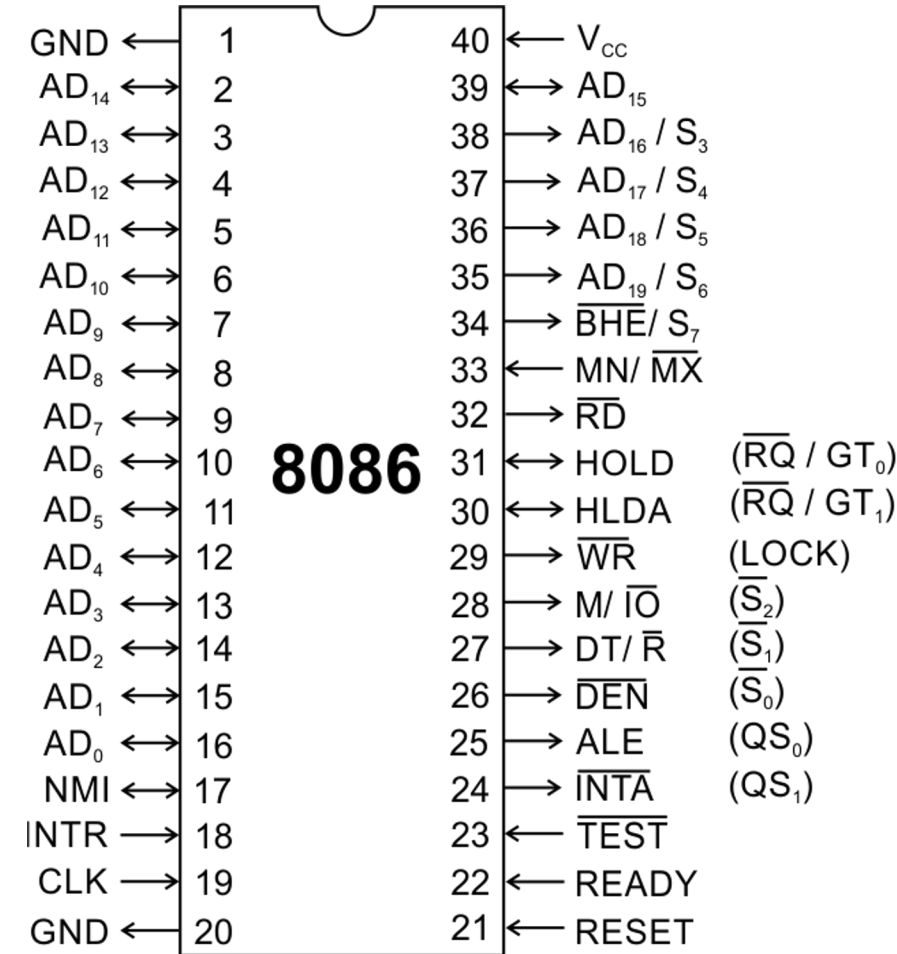
Power Supply Requirements

- Both microprocessors require +5.0 V with a supply voltage tolerance of ± 10 percent.
 - 8086 uses a maximum supply current of 360 mA
- Both microprocessors operate in ambient temperatures of between 0°C and 80°C .
- 80C86 is a **CMOS version** that requires only **10 mA** of power supply current.
 - and function in temperature extremes of -40°C through $+200^{\circ}\text{C}$



Pin Connections AD_{15} - AD_8

- 8086 **address/data bus** lines compose upper multiplexed address/data bus on the 8086.
- These lines contain address bits A_{15} – A_8 whenever **ALE** is a logic 1, and data bus connections D_{15} – D_8 when **ALE** is a logic 0.
- These pins enter a **high-impedance state** when a hold acknowledge occurs.



Pin Connections $A_{19}/S_6 - A_{16}/S_3$

- **Address/status bus** bits are multiplexed to provide address signals $A_{19}-A_{16}$ and **status bits** S_6-S_3 .
 - high-impedance state during **hold acknowledge**
 - status bit S_6 is always logic 0,
 - bit S_5 indicates the condition of the IF flag bit
- S_4 and S_3 show which segment is accessed during the current bus cycle.
 - these **status bits** can address four separate 1M byte memory banks by decoding as A_{21} and A_{20}

Pin Connections \overline{RD}

- When **read signal** is logic 0, the data bus is receptive to data from memory or I/O devices
 - pin floats high-impedance state during a hold acknowledge

Ready

- **Inserts wait states into the timing.**
 - if placed at a logic 0, the microprocessor enters into wait states and remains idle
 - if logic 1, no effect on the operation

Pin Connections INTR

- **Interrupt request** is used to request a hardware interrupt.
 - If INTR is held high when $IF = 1$, 8086 enters an interrupt acknowledge cycle after the current instruction has completed execution

NMI

- The **non-maskable interrupt** input is similar to INTR.
 - does not check IF flag bit for logic 1
 - if activated, uses interrupt vector 2

Pin Connections $\overline{\text{TEST}}$

- The $\overline{\text{Test}}$ pin is an input that is tested by the WAIT instruction.
- If $\overline{\text{TEST}}$ is a logic 0, the WAIT instruction functions as an NOP.
- If $\overline{\text{TEST}}$ is a logic 1, the WAIT instruction waits for **TEST** to become a logic $\overline{0}$.
- The **TEST** pin is most often connected to the 8087 numeric coprocessor.

Pin Connections RESET

- Causes the microprocessor to reset itself if held high a minimum of four clocking periods.
 - when 8086 is reset, it executes instructions at memory location FFFF0H
 - also disables future interrupts by clearing IF flag

CLK

- The **clock** pin provides the **basic timing signal**.
 - must have a duty cycle of 33 % (high for one third of clocking period, low for two thirds) to provide proper internal timing

Pin Connections VCC

- This **power supply** input provides a **+5.0 V**, **±10 %** signal to the microprocessor.

GND

- The **ground** connection is the return for the power supply.
 - 8086 microprocessors have two pins labeled GND—both must be connected to ground for proper operation

Pin Connections $\overline{MN/MX}$

- **Minimum/maximum** mode pin selects either minimum or maximum mode operation.
 - if minimum mode selected, the $\overline{MN/MX}$ pin must be connected directly to +5.0 V

BHE S_7

- The **bus high enable** pin is used in 8086 to enable the most-significant data bus bits (D_{15} – D_8) during a read or a write operation.
- The state of S_7 is always a logic 1.

Minimum Mode Pins

- Minimum mode operation is obtained by connecting the MN/MX pin directly to +5.0 V.
 - do not connect to +5.0 V through a pull-up register; it will not function correctly

M/ $\overline{\text{IO}}$

- The **M/ $\overline{\text{IO}}$** (8086) pin **selects** memory or I/O.
 - indicates the address bus contains either a memory address or an I/O port address.
 - **high-impedance state** during **hold acknowledge**

Minimum Mode Pins

WR

- **Write line** indicates 8086 is outputting data to a memory or I/O device.
 - during the time \overline{WR} is a logic 0, the data bus contains valid data for memory or I/O
 - high-impedance during a hold acknowledge

INTA

- The **interrupt acknowledge** signal is a response to the **INTR** input pin.
 - normally used to gate the interrupt vector number onto the data bus in response to an interrupt

Minimum Mode Pins ALE

- **Address latch enable** shows the 8086 address/data bus contains an address.
 - can be a memory address or an I/O port number
 - ALE signal doesn't float during hold acknowledge

DT/ \overline{R}

- The **data transmit/receive** signal shows that the microprocessor data bus is transmitting (**DT/ \overline{R} = 1**) or receiving (**DT/ \overline{R} = 0**) data.
 - used to enable external data bus buffers

Minimum Mode Pins DEN

- **Data bus enable** activates external data bus buffers.

HOLD

- **Hold input** requests a direct memory access (DMA).
 - if **HOLD** signal is a logic **1**, the microprocessor stops executing software and places address, data, and control bus at **high-impedance**
 - if a logic 0, software executes normally

Minimum Mode Pins HLDA

- **Hold acknowledge** indicates the 8086 has entered the **hold state**.

$\overline{SS0}$

- The $\overline{SS0}$ status line is **equivalent** to the S_0 pin in maximum mode operation.
- **Signal** is combined with $\overline{IO/\overline{M}}$ and $\overline{DT/\overline{R}}$ to decode the function of the current bus cycle.

Maximum Mode Pins

- In order to achieve maximum mode for use with external coprocessors, connect the MN/ \overline{MX} pin to **ground**.

$\overline{S2}$, $\overline{S1}$, and $\overline{S0}$

- **Status bits** indicate function of the current bus cycle.
 - normally decoded by the 8288 bus controller

Maximum Mode Pins $\overline{\text{RQ}}/\overline{\text{GT}}1$

- The **request/grant** pins request direct memory accesses (DMA) during maximum mode operation.
 - bidirectional; used to request and grant a DMA operation

$\overline{\text{LOCK}}$

- The **lock** output is used to lock peripherals off the system. This pin is activated by using the `LOCK:` prefix on any instruction.

Maximum Mode Pins QS₁ and QS₀

- The **queue status bits** show the status of the internal instruction queue.
 - provided for access by the 8087 coprocessor

Queue status		Queue operation
QS ₁	QS ₀	
0	0	No operation
0	1	First byte of an opcode from queue
1	0	Empty the queue
1	1	Subsequent byte from queue

BUS BUFFERING AND LATCHING

- Before 8086 can be used with memory or I/O interfaces, their **multiplexed buses** must be **demultiplexed**.
- This section provides detail required to demultiplex the buses and illustrates how the **buses** are buffered for very large systems.
 - because the maximum fan-out is 10, the system must be buffered if it contains more than 10 other components

Demultiplexing the Buses

- The **address/data** bus of the 8086 is **multiplexed** (shared) to reduce the number of pins required for the integrated circuit
 - the hardware designer must **extract** or **demultiplex** information from these pins
- Memory & I/O require the address remain valid and stable throughout a read/write cycle.
- If buses are **multiplexed**, the address changes at the memory and I/O, causing them to read or write data in the wrong locations

- All computer systems have **three buses**:
 - an **address bus** that provides memory and I/O with the memory address or the I/O port number
 - a **data bus** that transfers data between the microprocessor and the memory and I/O
 - a **control bus** that provides control signals to the memory and I/O
- These buses must be present in order to interface to memory and I/O.

Demultiplexing the 8086

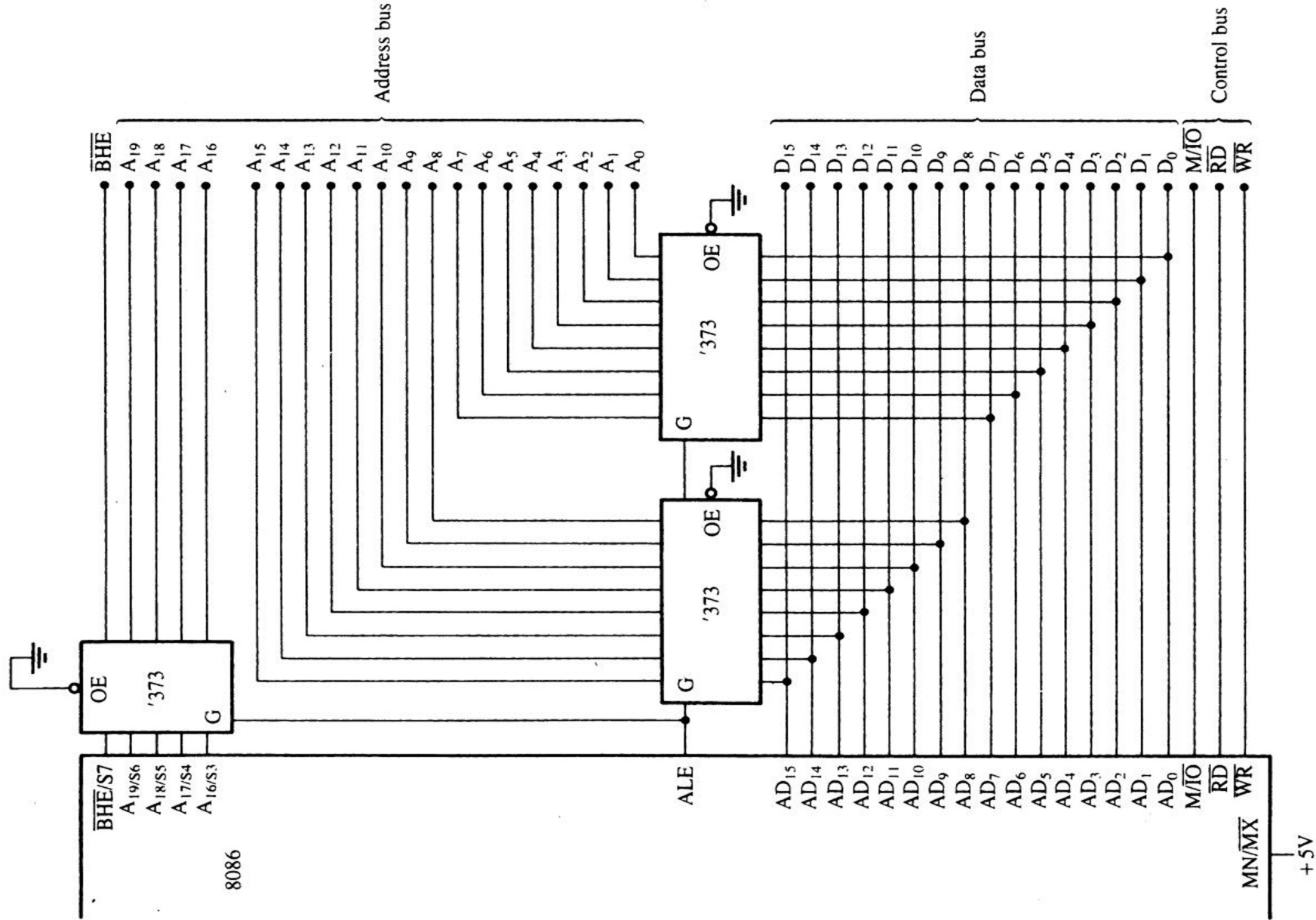
- Figure 2 illustrates components required to demultiplex 8086 buses.
 - three 74LS373 or 74LS573 **transparent latches** are used to demultiplex the address/data bus connections $AD_{15}-AD_0$
 - and address/status connections $A_{19}/S_6-A_{16}/S_3$
- The latches, which are like **wires** whenever the **Address Latch Enable** pin (**ALE**) becomes a logic 1, pass the inputs to the outputs.

- After a short time, ALE returns to logic 0 causing the latches to remember inputs at the time of the change to a logic 0.
- This yields a **separate address bus** with connections A_{19} – A_0 .
 - these allow 8086 to address 1Mb of memory
- The **separate data bus** allows it to be connected to any 8-bit peripheral device or memory component.

Demultiplexing the 8086

- Fig 2 illustrates a demultiplexed 8086 with all three buses:
- **address** ($A_{19}-A_0$ and \overline{BHE})
- **data** ($D_{15}-D_0$),
- **control** (M/\overline{IO} , \overline{RD} , and \overline{WR})
- Here, the memory and I/O system see the 8086 as a device with:
 - a **20-bit address bus**; **16-bit data bus**
 - and a **three-line control bus**

Figure 2 The 8086 microprocessor shown with a demultiplexed address bus. This is the model used to build many 8086-based systems.



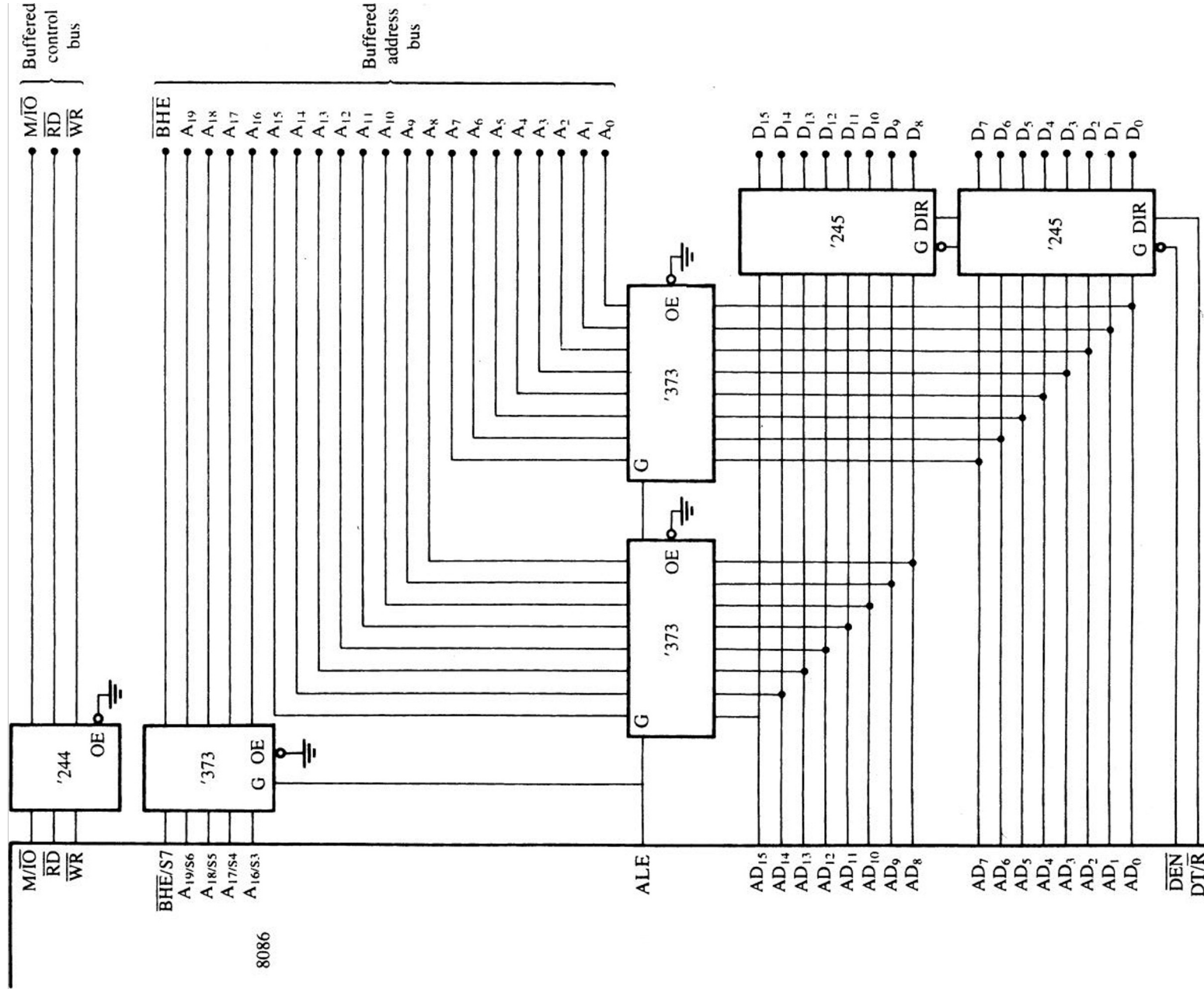
The Buffered System

- If more than 10 unit loads are attached to any bus pin, the entire system must be **buffered**.
- Buffer output currents have been increased so that more TTL unit loads may be driven.
- A fully buffered signal will introduce a **timing delay** to the system.
- No difficulty unless memory or I/O devices are used which function at near **maximum bus speed**.

The Fully Buffered 8086

- Figure 3 illustrates a **fully buffered** 8086.
 - a fully buffered 8086 system requires **one** 74LS244, **two** 74LS245s, and **three** 74LS373s
- **Direction** of the 74LS245 is controlled by the **DT/ \overline{R}** signal.
 - **enabled** and disabled by the **\overline{DEN}** signal
- It also has a **\overline{BHE}** signal that is buffered for **memory-bank selection**.

Figure 3 A fully buffered 8086 microprocessor.



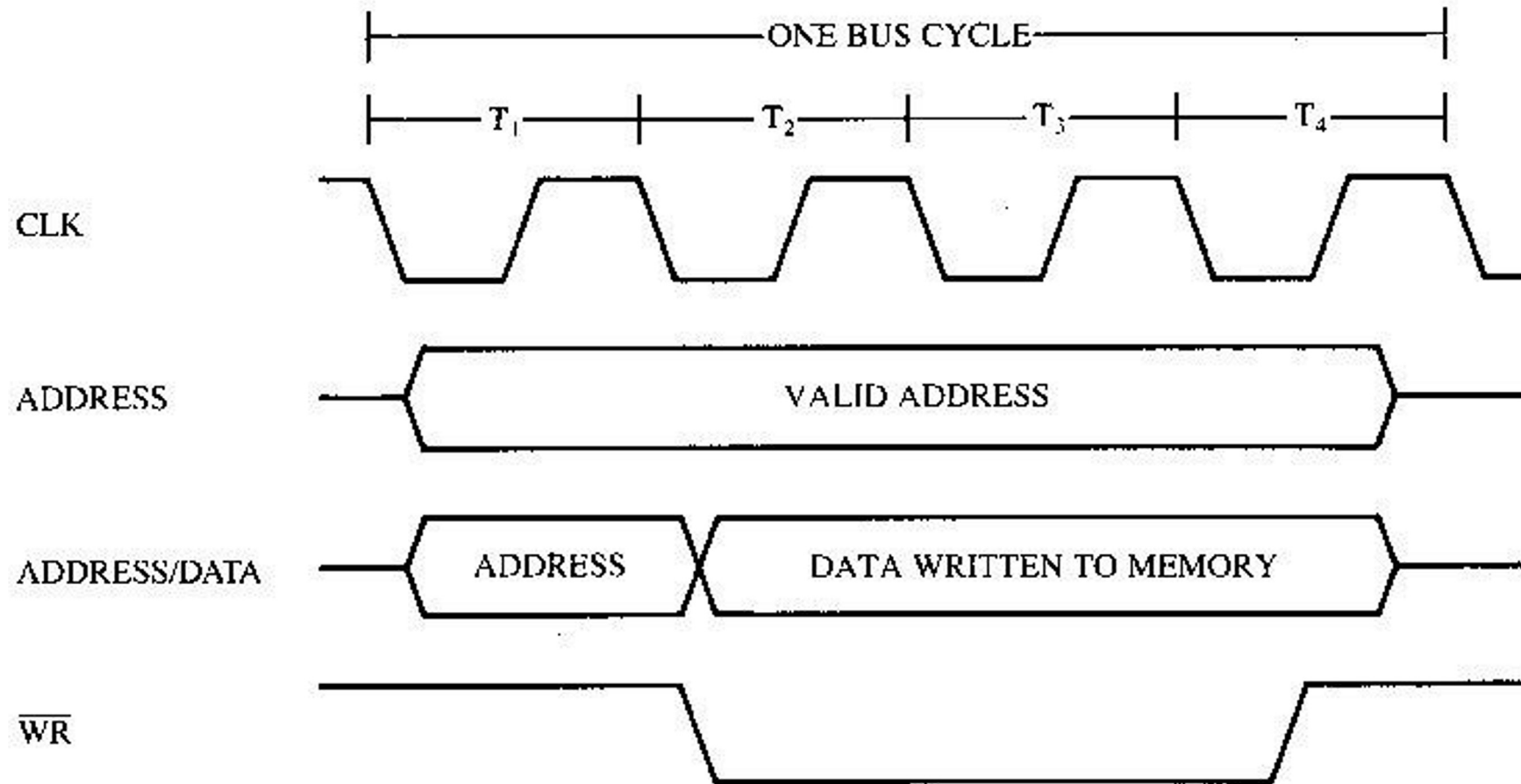
BUS TIMING

- It is essential to understand system **bus timing** before choosing memory or I/O devices for interfacing to 8086 microprocessors.
- This section provides insight into operation of the bus signals and the **basic read/write timing** of the 8086.

Basic Bus Operation

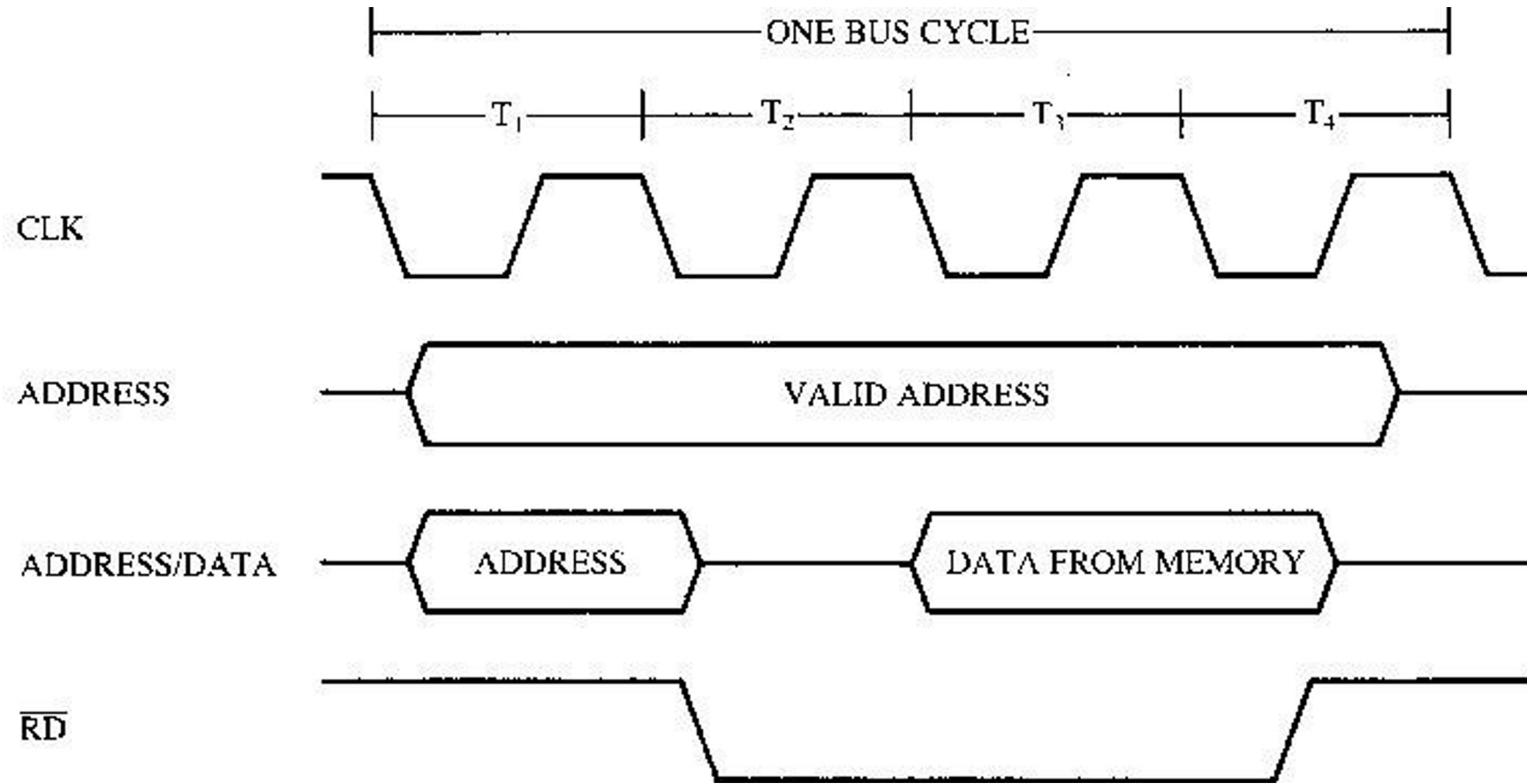
- The three buses of 8086 function the same way as any other microprocessor.
- If data are **written to memory** the processor:
 - **outputs** the memory address on the address bus
 - **outputs** the data to be written on the data bus
 - **issues** a write (\overline{WR}) to memory
 - and $\overline{IO}/M = 0$ for peripheral and $\overline{IO}/M = 1$ for writing in a memory
- See simplified timing for write in Fig 4.

Figure 4 Simplified 8086 **write bus cycle**.



- If data are read from the memory the microprocessor:
 - **outputs** the memory address on the address bus
 - **issues** a **read** memory signal (\overline{RD})
 - and **accepts** the data via the data bus
- See simplified timing for read in Fig 5.

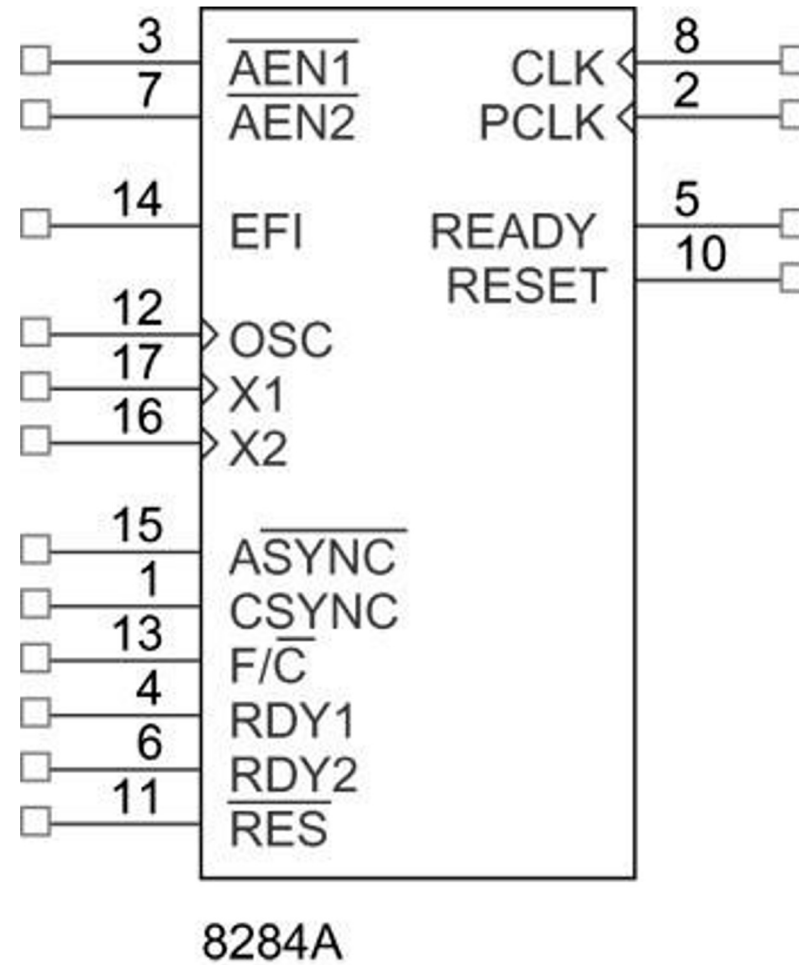
Figure 5 Simplified 8086 read bus cycle.



CLOCK GENERATOR (8284A)

- This section describes the 8284A clock generator and the **RESET** signal.
 - also introduces the **READY** signal for 8086
- With no clock generator, many circuits would be required to generate the clock (CLK).
- 8284A provides the following basic functions:
 - clock generation; RESET & READY synch;
 - TTL-level peripheral clock signal
- Figure 6 shows **pin-outs** of the 8284A

Figure 6 The pin-out of the 8284A clock generator.



8284A *Pin Functions*

- 8284A is an 18-pin integrated circuit designed specifically for use 8086.

$\overline{\text{AEN1}}$ and $\overline{\text{AEN2}}$

- The **address enable** pins are provided to qualify bus ready signals, RDY1 and RDY2.
 - used to cause wait states
- **Wait states** are generated by the **READY** pin of 8086 controlled by these two inputs.

Pin Functions RDY₁ and RDY₂

- The **bus ready** inputs are provided, in conjunction with the $\overline{\text{AEN1}}$ & $\overline{\text{AEN2}}$ pins, to cause wait states in 8086.

$\overline{\text{ASYNC}}$

- The **ready synchronization** selection input selects either one or two stages of synchronization for the RDY₁ and RDY₂ inputs.

Pin Functions READY

- **8284 Ready** is an output pin that connects to the 8086 READY input.
 - synchronized with the RDY₁ and RDY₂ inputs

X₁ and **X₂**

- The **crystal oscillator** pins connect to an external crystal used as the timing source for the clock generator and all its functions

Pin Functions F/ \bar{C}

- The **frequency/crystal** select input chooses the clocking source for the 8284A.
 - if held high, an **external clock** is provided to the EFl input pin
 - if held low, the **internal crystal oscillator** provides the timing signal
- The e external frequency input is used when the **F/C** pin is pulled high.
- EFl supplies timing when the **F/ \bar{C}** pin is high.

Pin Functions CLK

- The **clock output** pin provides the CLK input signal to 8086 and other components.
 - output signal is one third of the crystal or EFI input frequency
 - 33% duty cycle required by the 8086

PCLK

- The **peripheral clock** signal is one sixth the crystal or EFI input frequency.
 - PCLK output provides a clock signal to the peripheral equipment in the system

Pin Functions OSC

- **Oscillator output** is a TTL-level signal at the same frequency as crystal or EFI input.
 - OSC output provides EFI input to other 8284A clock generators in multiple-processor systems

RES

- **Reset input** is an active-low input to 8284A.
 - often connected to an RC network that provides power-on resetting

Pin Functions RESET

- **Reset output** is connected to the 8086 RESET input pin.

CSYNCH

- The **clock synchronization** pin is used when the EFI input provides synchronization in systems with multiple processors.
 - if internal crystal oscillator is used, this pin must be grounded

Pin Functions

GND

- The **ground pin** connects to ground.

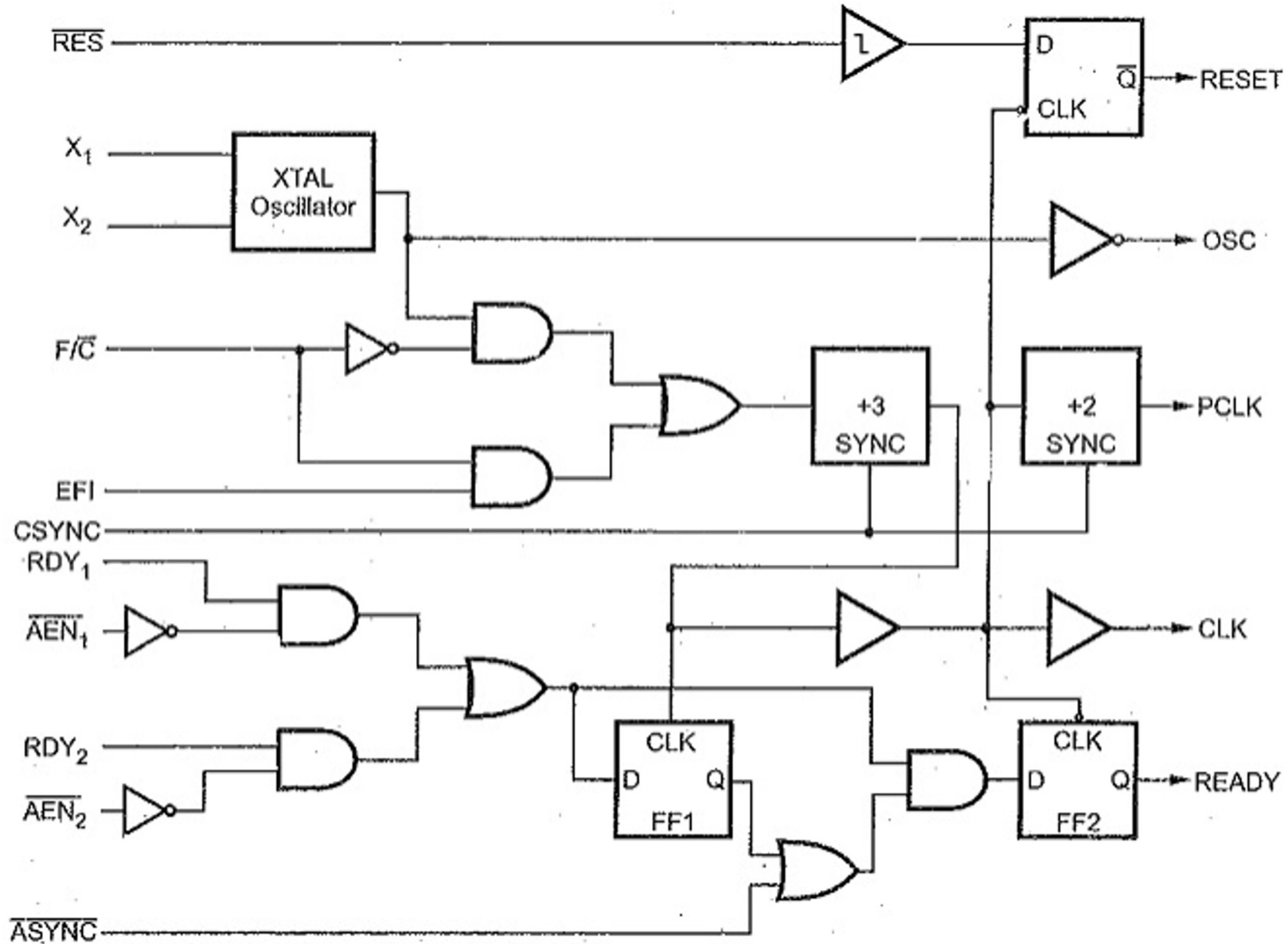
VCC

- This **power supply** pin connects to +5.0 V with a tolerance of $\pm 10\%$.

Operation of the 8284A

- The 8284A is a relatively easy component to understand.
- Figure 7 illustrates the internal timing diagram of the 8284A clock generator.
- The top half of the logic diagram represents the clock and synchronization section of the 8284A clock generator.

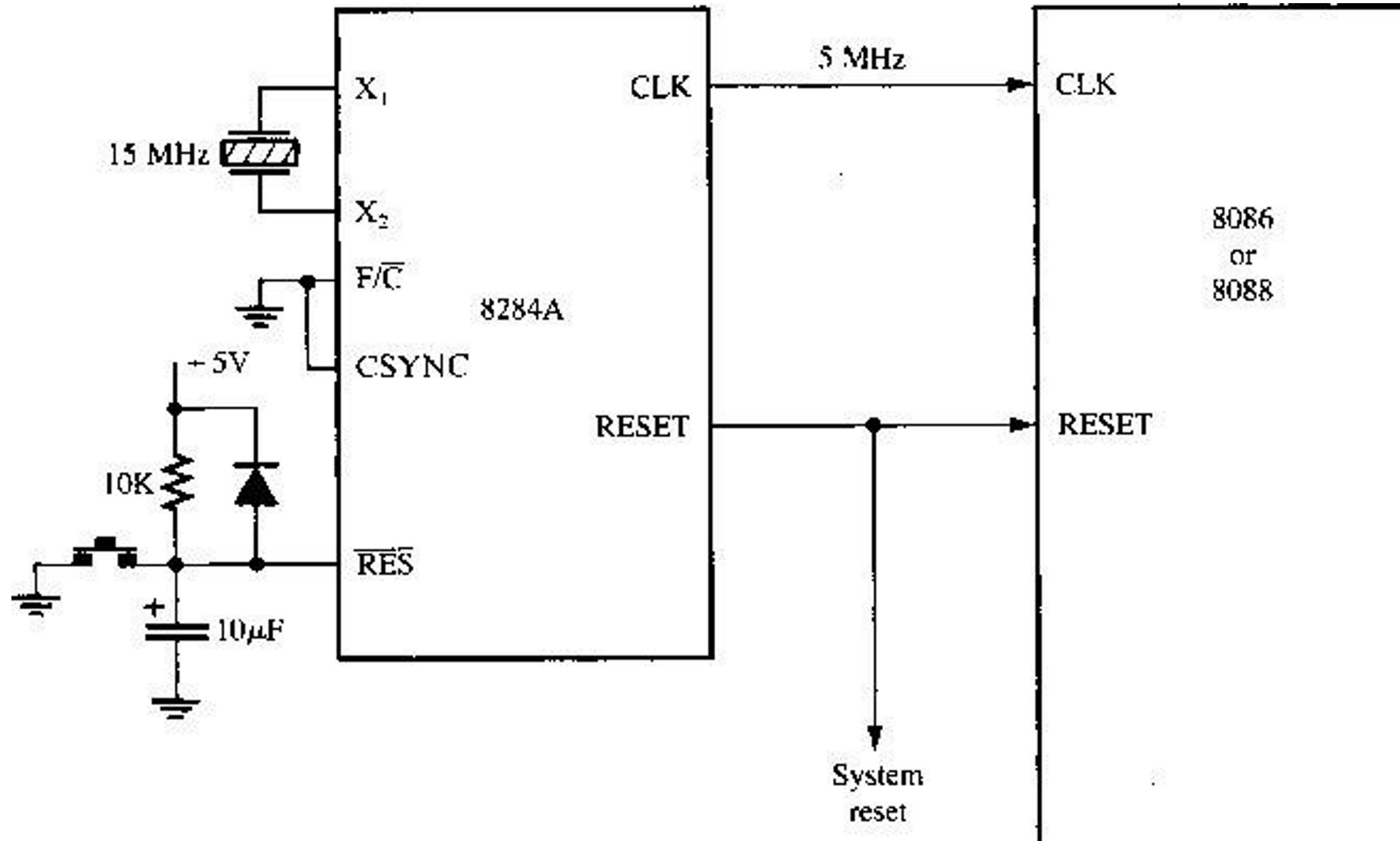
Figure 7 The internal block diagram of the 8284A clock generator.



Operation of the Clock Section

- Crystal oscillator has two inputs: X_1 and X_2 .
 - if a crystal is attached to X_1 and X_2 , the oscillator generates a square-wave signal at the same frequency as the crystal
- The square-wave is fed to an AND gate & an inverting buffer to provide an OSC output.
- The OSC signal is sometimes used as an EFl input to other 8284A circuits in a system.
- Figure 8 shows how an 8284A is connected to the 8086/8088.

Figure 8 The clock generator (8284A) and the 8086 microprocessor illustrating the connection for the clock and reset signals. A 15 MHz crystal provides the 5 MHz clock for the microprocessor.



Operation of the Reset Section

- The reset section of 8284A consists of a **Schmitt trigger buffer** and a **D-type flip-flop**.
 - the D-type flip-flop ensures timing requirements of 8086/8088 RESET input are met
- This circuit applies the RESET signal on the **negative edge (1-to-0 transition)** of each clock.
- 8086 microprocessors sample RESET at the **positive edge (0-to-1 transition)** clocks.
 - thus, this circuit meets 8086 timing requirements

RDY and the 8284A

- RDY is the synchronized ready input to the 8284A clock generator.
- Internal 8284A circuitry guarantees the **accuracy** of the READY synchronization.

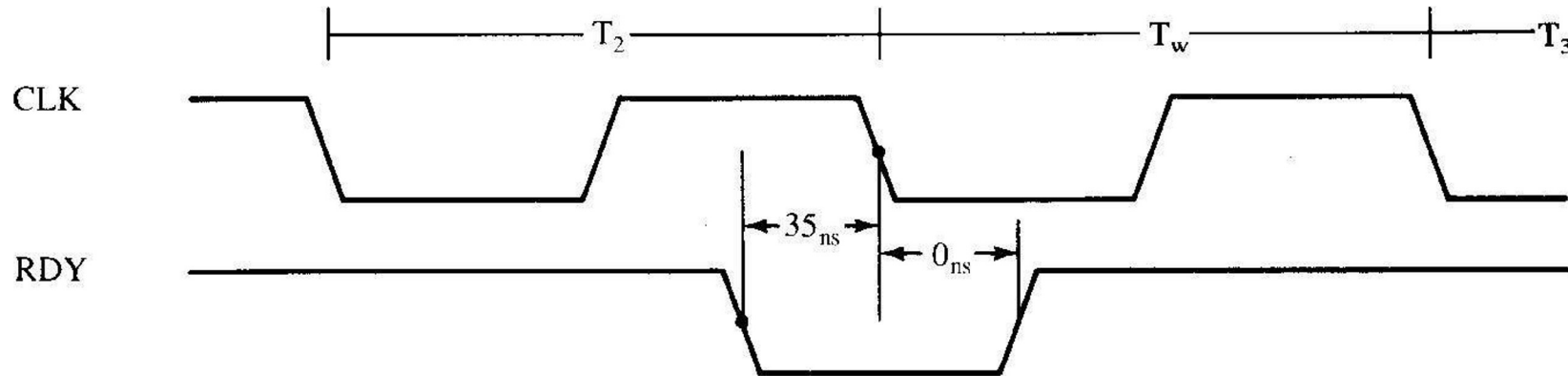
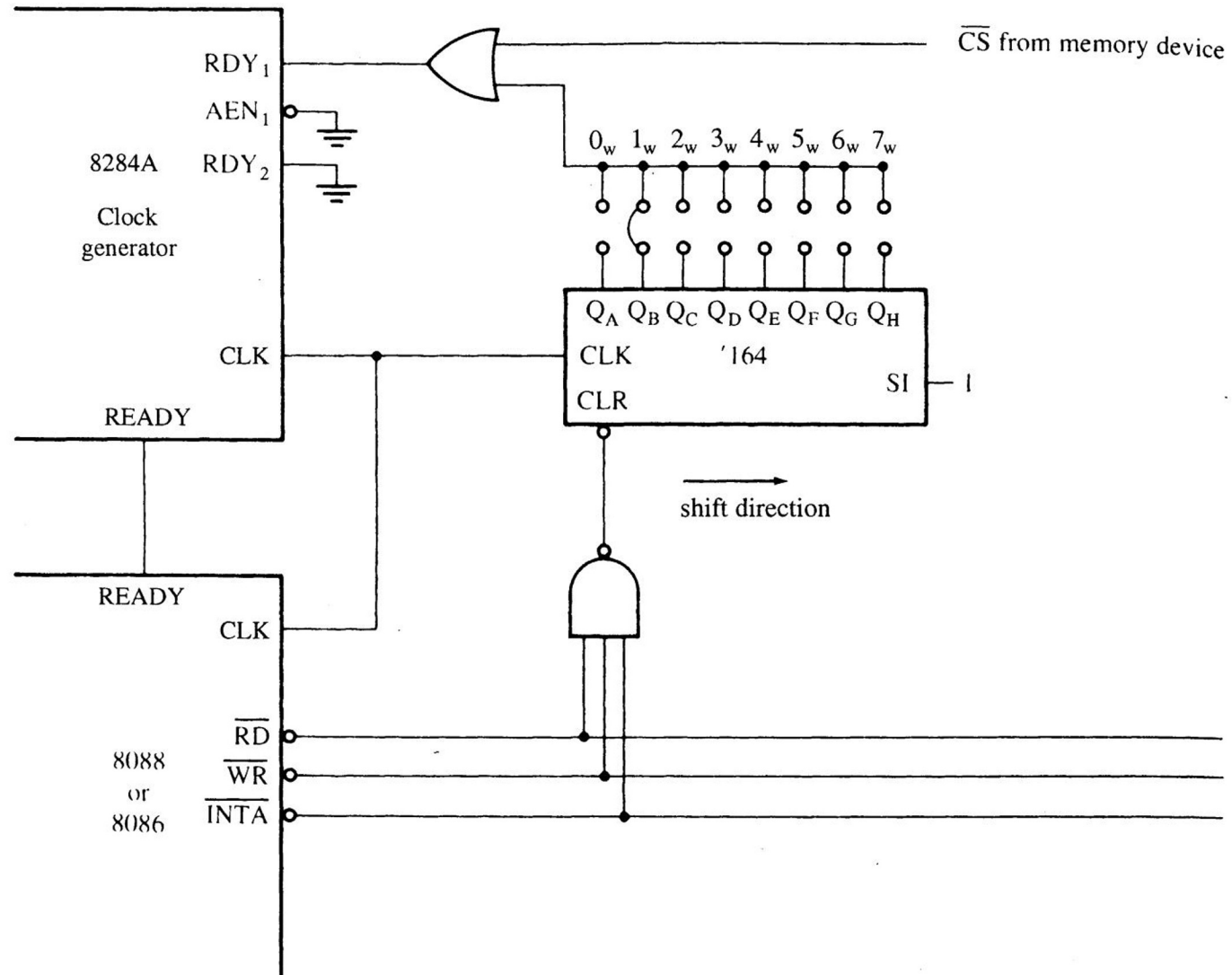


Figure 9 8284A RDY input timing.

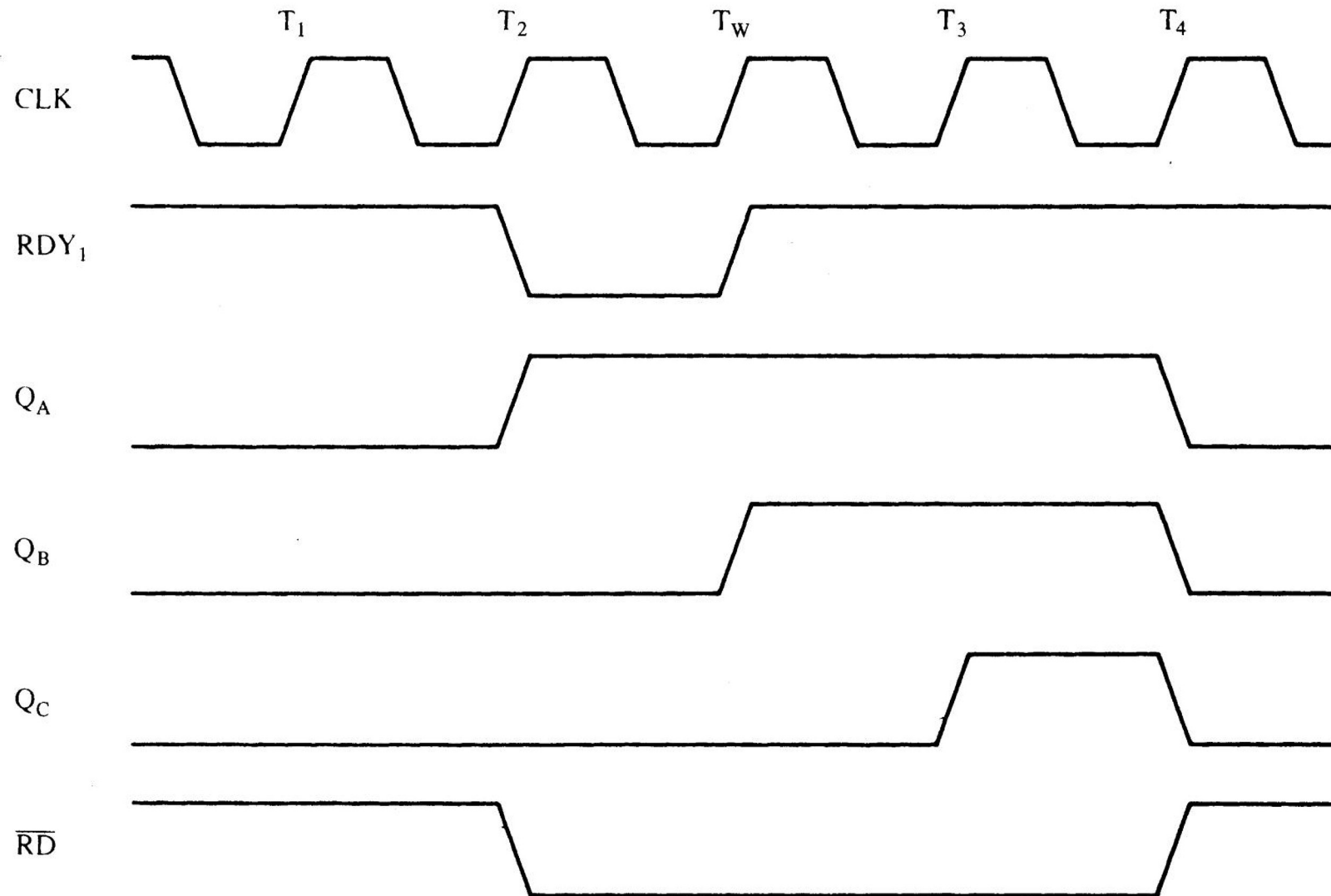
- Fig 7 depicts internal structure of 8284A.
 - the bottom half is the READY synch circuitry
- Fig 10 shows a circuit to introduce almost any number of wait states to 8086/8088.
- An 8-bit serial **shift** register (74LS164) shifts a logic 0 for one or more clock periods from one of its Q outputs through to the RDY1 input of the 8284A.
- With appropriate strapping, this circuit can provide **various numbers** of wait states.

Figure 10 A circuit that will cause between 0 and 7 wait states.



- Note in Fig 10 that this circuit is **enabled** only for devices that need **insertion of waits**.
 - if the selection signal is a logic 0, the device is selected and this circuit generates a wait state
- Figure 11 shows timing of this **shift register** wait state generator when wired to insert one wait state.
- The timing diagram also illustrates the internal contents of the shift register's flip-flops
 - to present a more detailed view of its operation
- In this example, **one wait state** is generated.

Figure 11 Wait state generation timing of the circuit of Figure 10



MINIMUM VS MAXIMUM MODE

- **Minimum mode** is obtained by connecting the mode selection $\overline{MN/MX}$ pin to **+5.0 V**,
 - maximum mode selected by grounding the pin
- The mode of operation provided by minimum mode is similar to that of the 8085A
 - the most recent Intel 8-bit microprocessor
- Maximum mode is designed to be used whenever a **coprocessor** exists in a system.
 - maximum mode was dropped with 80286

Minimum Mode Operation

- Least expensive way to operate 8086.
 - because all control signals for the memory & I/O are generated by the microprocessor
- Control signals are identical to Intel 8085A.
- The **minimum mode** allows 8085A **8-bit peripherals** to be used with the 8086 without any special considerations.

Time in μP

- T-state is the smallest unit of time in a μp
- 1 clock cycle = 1 T-state
- In 8086, 1 machine cycle = 4 T-states
- 1 machine cycle (or bus cycle) is the time required to
 - T1 – send out an address – on address bus
 - T2 – send out a signal (read/ write) – on control bus
 - T3 – read/ write data on that location – on data bus
 - T4 – release all buses
- 1 instruction cycle = n machine cycles (depends on the instruction)

Timing in General

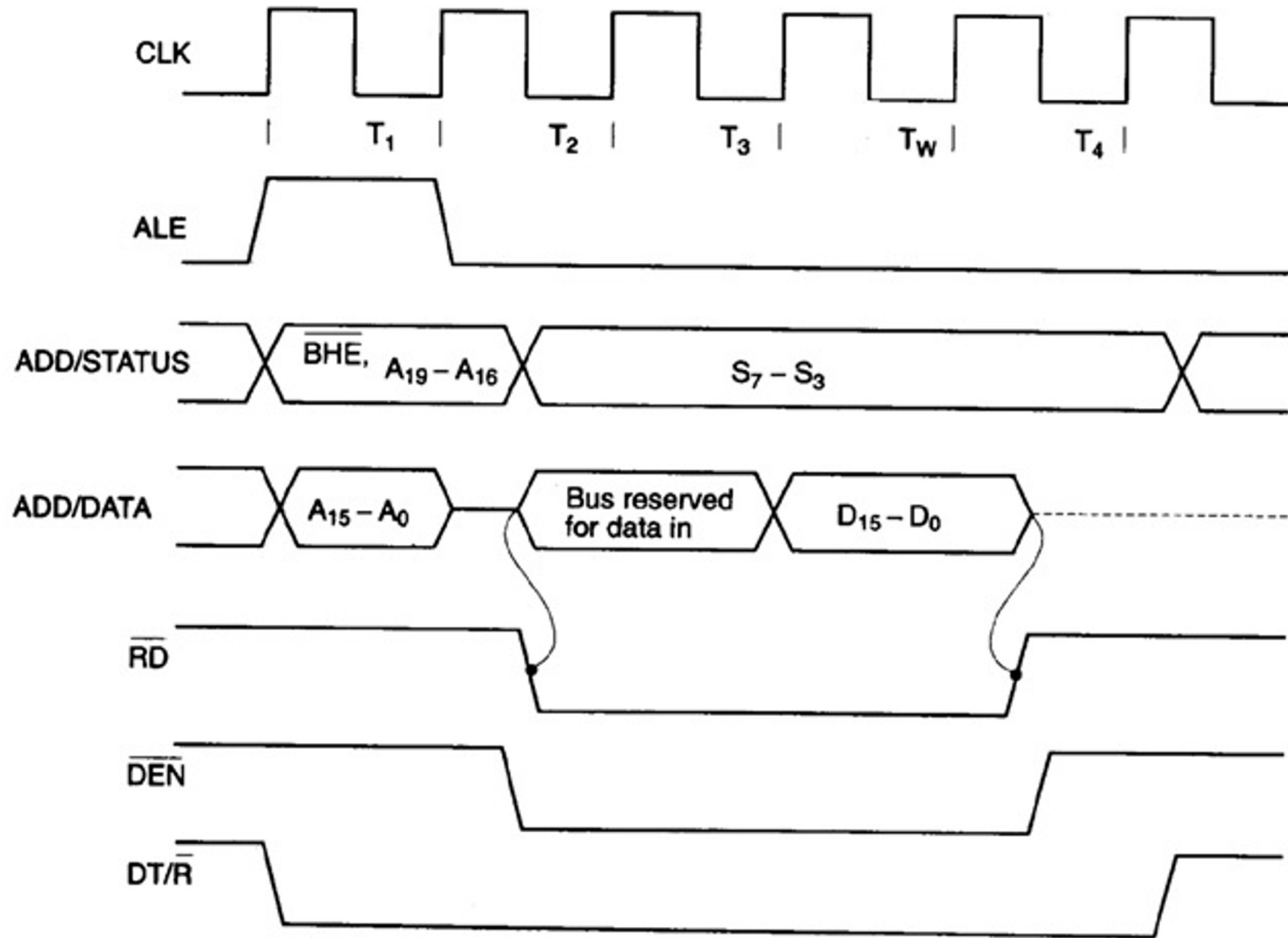
- 8086 use memory and I/O in periods called bus cycles.
- Each cycle equals **four** system-clocking periods (**T states**).
 - **newer** microprocessors divide the bus cycle into as few as **two** clocking periods
- If the clock is operated at 5 MHz, one 8086 bus cycle is complete in 800 ns.
 - basic operating frequency for these processors

- During the **first** clocking period in a bus cycle, called **T1**, many things happen:
 - the **address** of the memory or I/O location is sent out via the address bus and the address/data bus connections.
- During T1, **control signals** are also output.
 - indicating whether the address bus contains a memory address or an I/O device (port) number
- During **T2**, the processor issues the **RD** or **\overline{WR}** signal, **DEN**, and in the case of a write, the data to be written appears on the data bus.

- These events cause the memory or I/O device to begin to perform a read or a write.
- **READY is sampled** at the end of T_2 .
 - if low at this time, T_3 becomes a wait state (T_w)
 - this clocking period is provided to allow the memory time to access data
- If a read bus cycle, the data bus is sampled at the end of T_3 .
- Illustrated in Figure 12.

Figure 12
operation.

Minimum mode 8086 bus timing for a read operation.



- In T_4 , all bus signals are deactivated in preparation for the next bus cycle
- Data bus connections are sampled for data read from memory or I/O

Read Timing

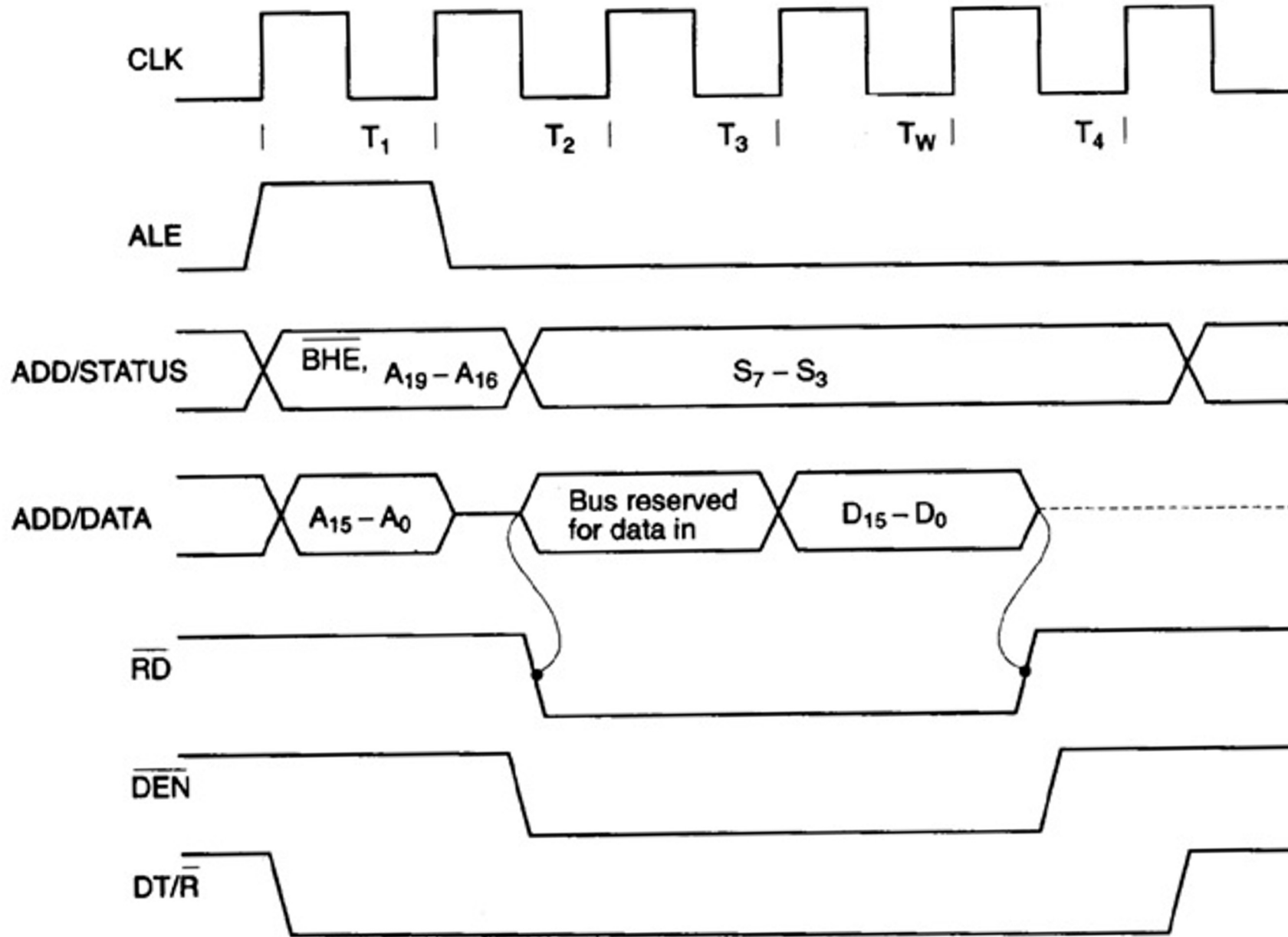
- Figure 12 depicts 8086 **read timing**.
- Important item in the read timing diagram is time allowed for memory & I/O to read data.
- Memory is chosen by its access time.
 - the fixed amount of time the microprocessor allows it to access data for the read operation
- It is extremely important that memory chosen complies with the limitations of the system.

Write Timing

- Figure 13 illustrates 8086 write-timing.
- The \overline{RD} strobe is replaced by the \overline{WR} strobe,
 - the data bus contains information *for* the memory rather than information *from* the memory,
 - DT/\overline{R} remains a logic 1 instead of a logic 0 throughout the bus cycle
- When interfacing some devices, timing may be **critical** between when \overline{WR} becomes logic 1 and the data are removed from the data bus.

Figure 13

Minimum mode 8086 write bus



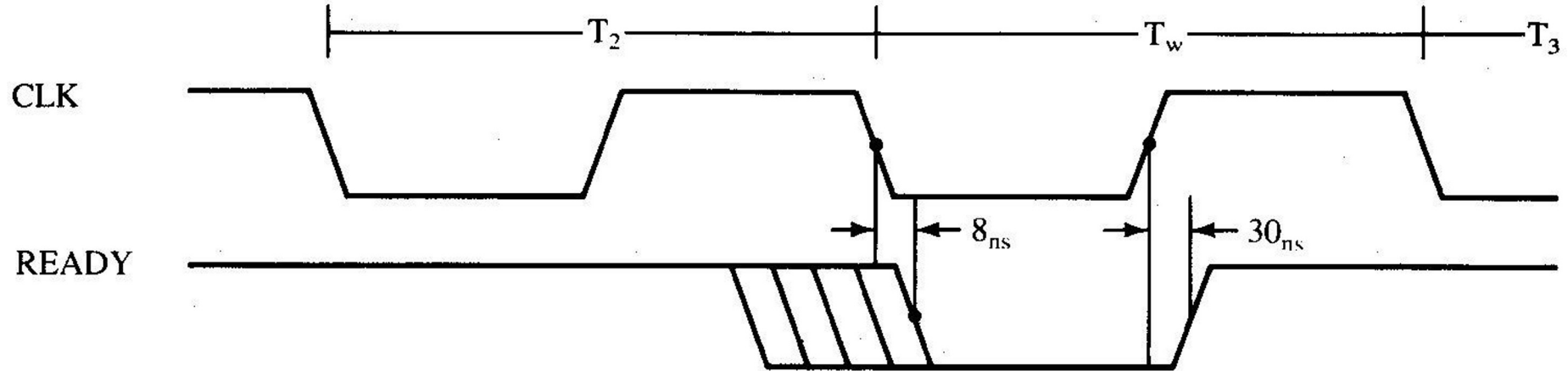
READY AND THE WAIT STATE

- The READY input causes wait states for slower memory and I/O components.
 - a **wait state** (T_w) is an extra clocking period between T_2 and T_3 to lengthen bus cycle
 - on **one wait state**, memory access time of **460 ns**, is lengthened by one clocking period (**200 ns**) to **660 ns**, based on a 5 MHz clock

The **READY** Input

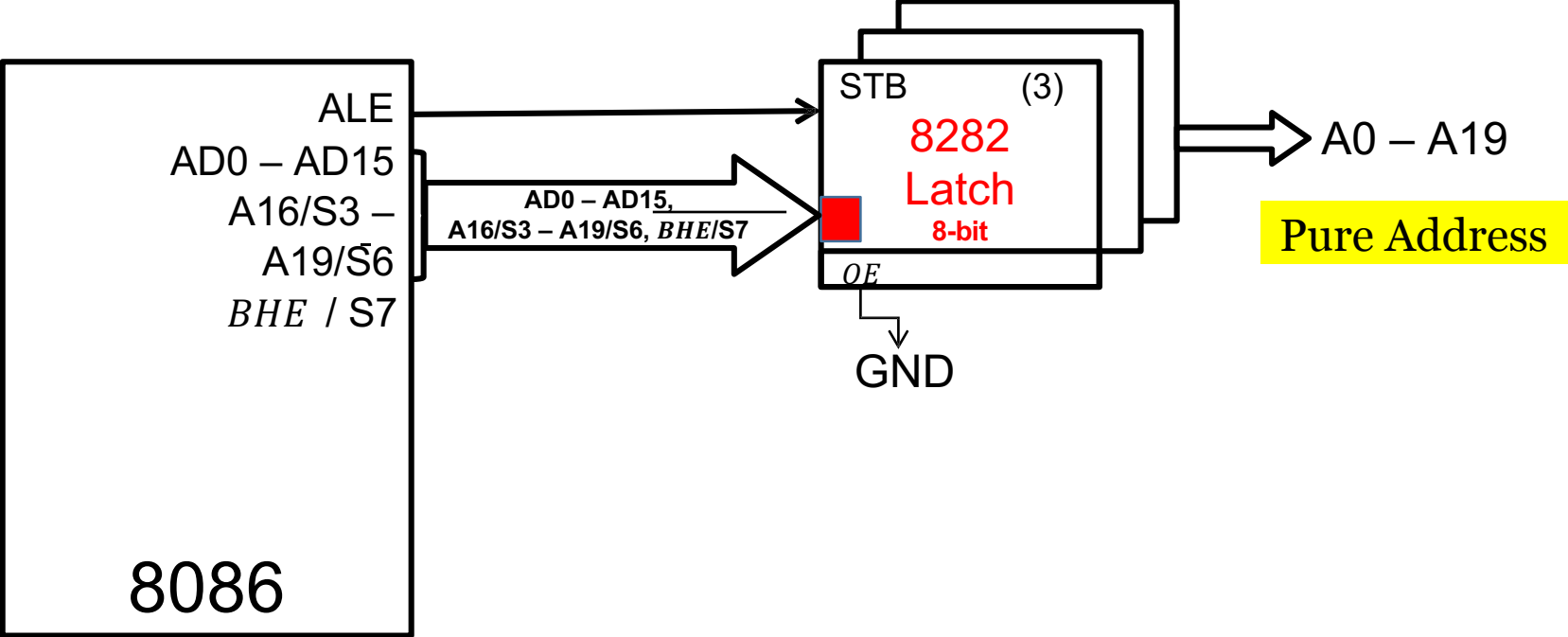
- The READY input is sampled at the end of T_2 and again, if applicable, in the middle of T_w .
- The READY input to 8086 has stringent timing requirements.
- Fig 14 shows READY causing one wait state (T_w), with the required setup and hold times from the system clock.

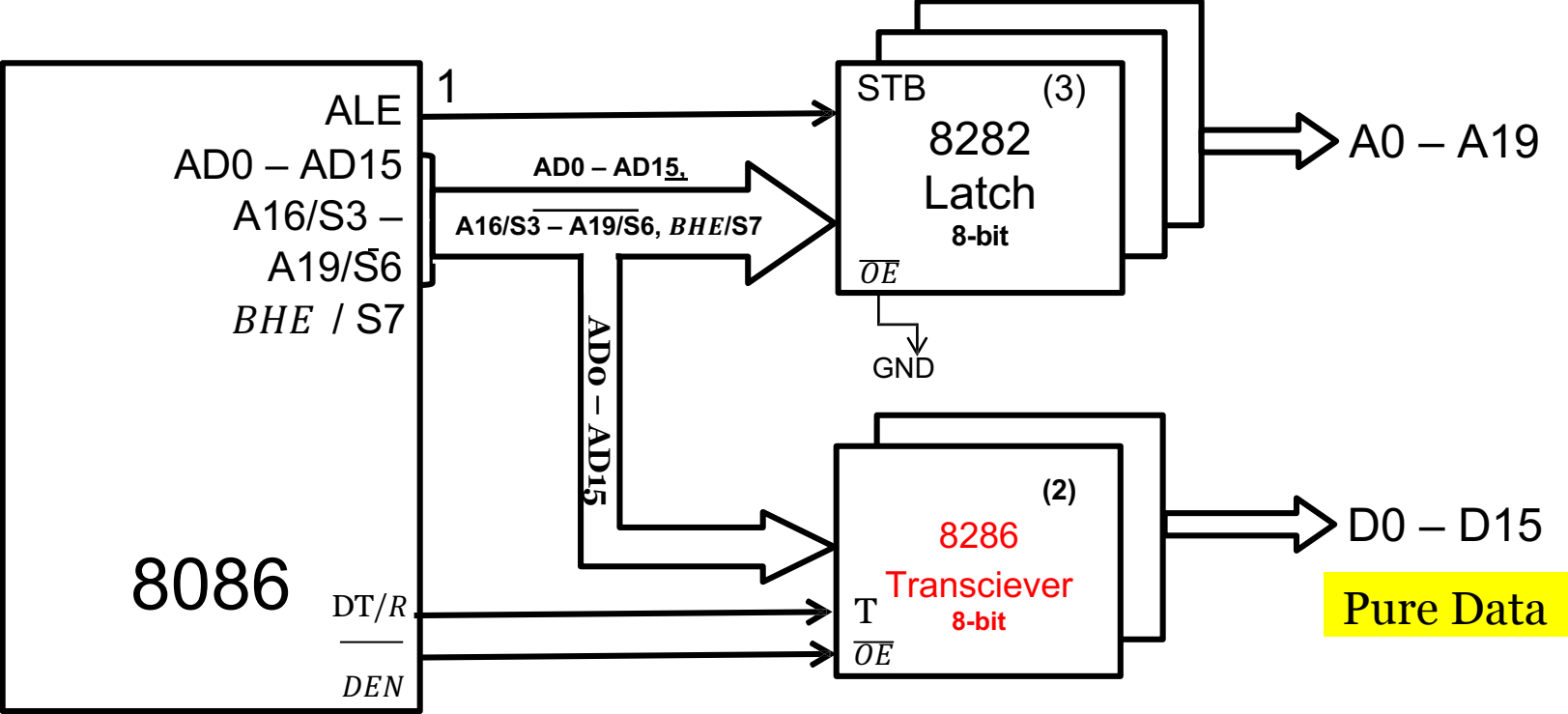
Figure 14 8086 READY input timing.

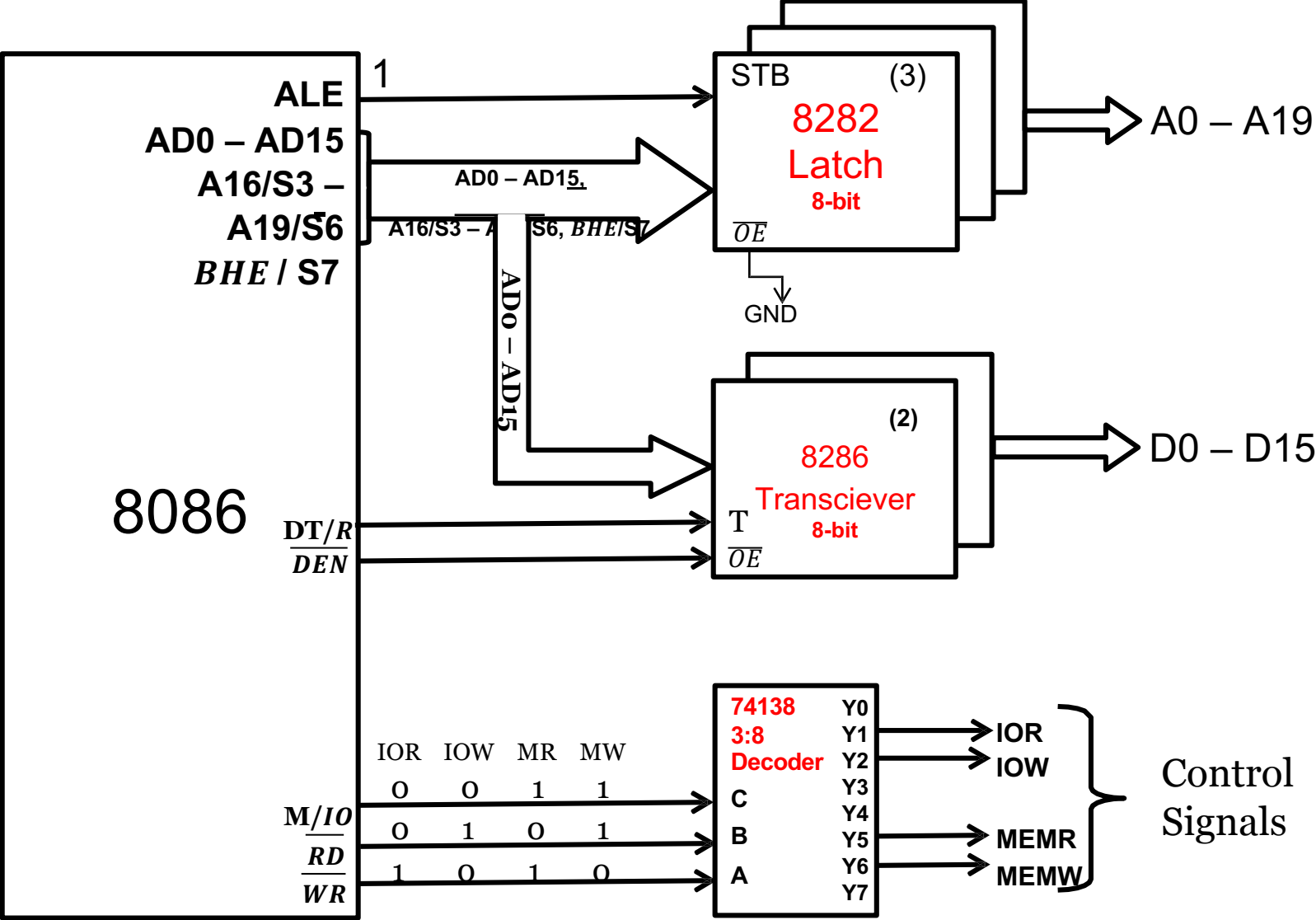


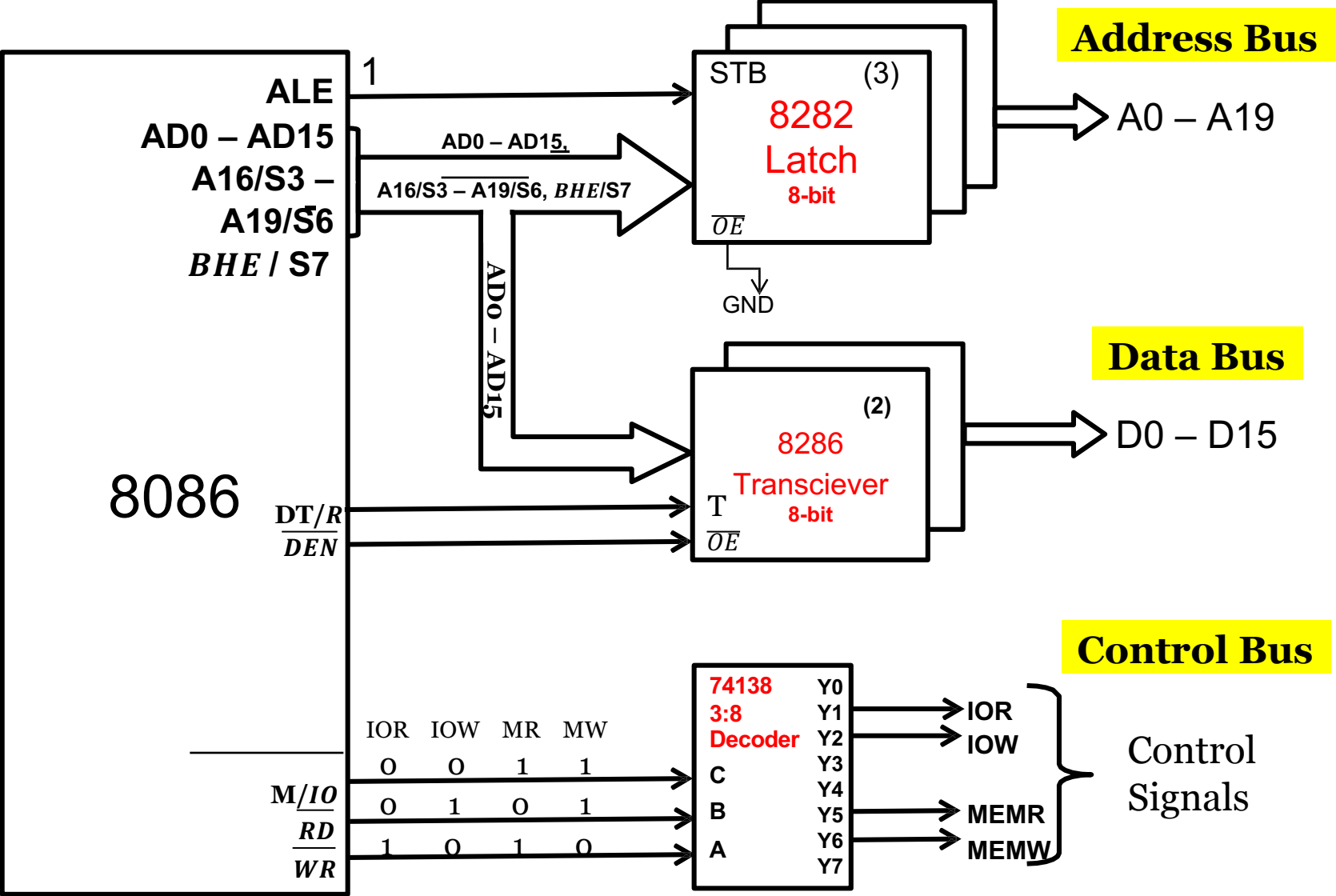
- If READY is logic 0 at the end of T_2 , T_3 is delayed and T_w inserted between T_2 and T_3 .
- READY is next sampled at the middle of T_w to determine if the next state is T_w or T_3 .

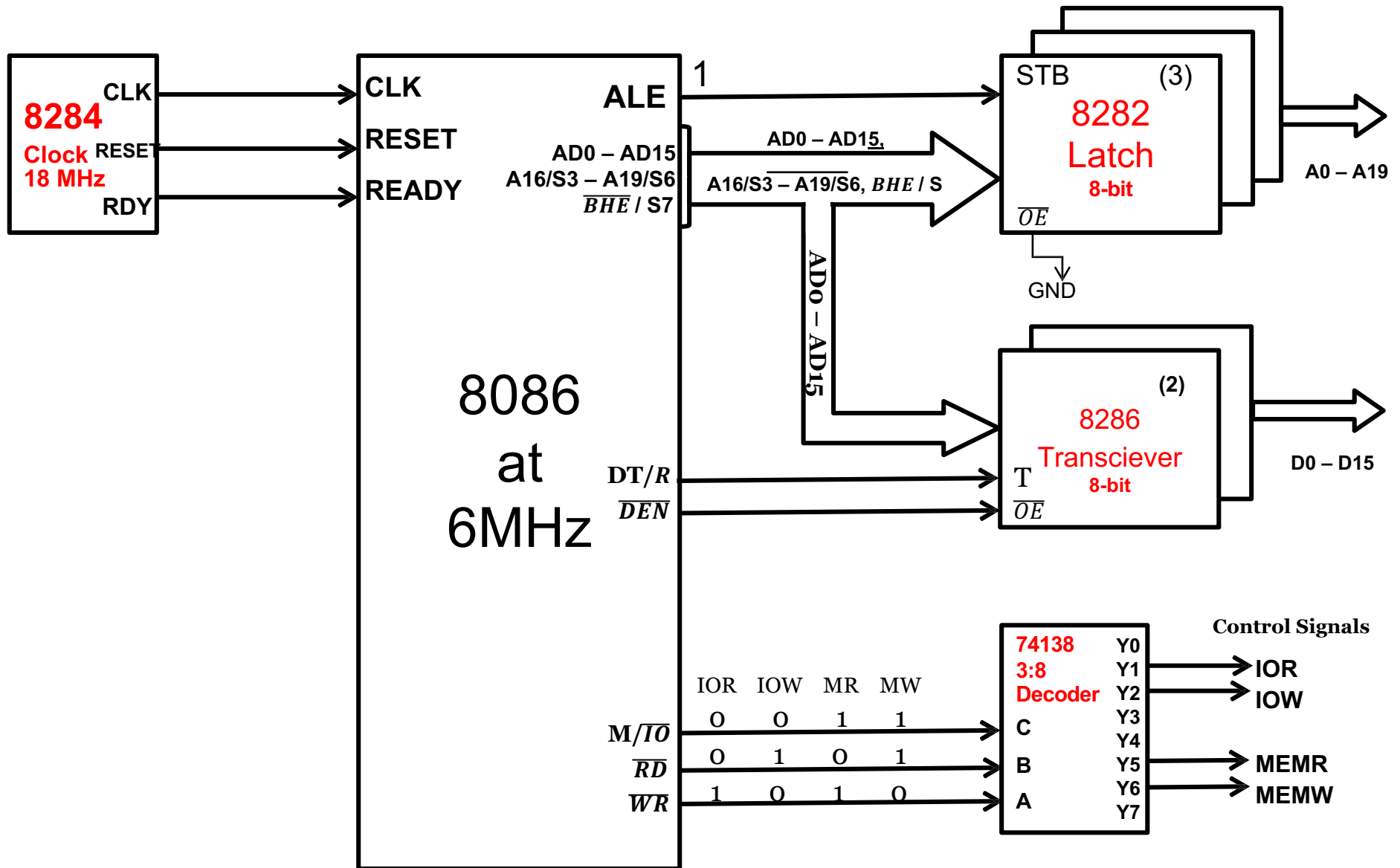
- The 8086 ALU sets the pins A0 – A19 to match the 20-bit address of the location it wants to access
- This value is not stored on these pins for a long time
- This value gets rewritten as D0 – D15 and status lines within the next fraction of a second
- Where is A0 – A19 after that?
- In the address bus!
- How to get pure address from AD0 – AD15? (Demultiplex)
- **By using a LATCH**
- to save only the address from these pins, and remain cut-off when data is on them.

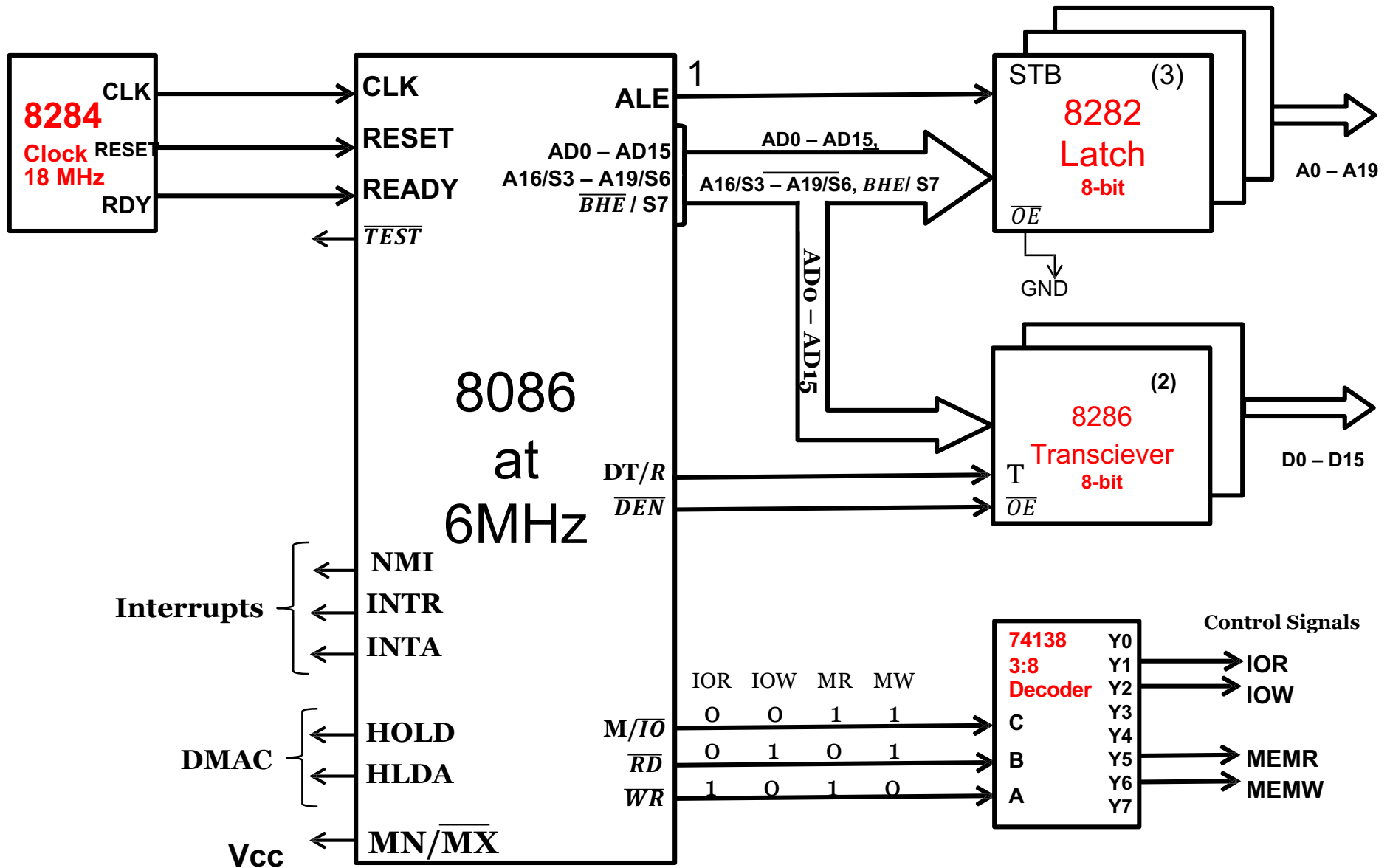




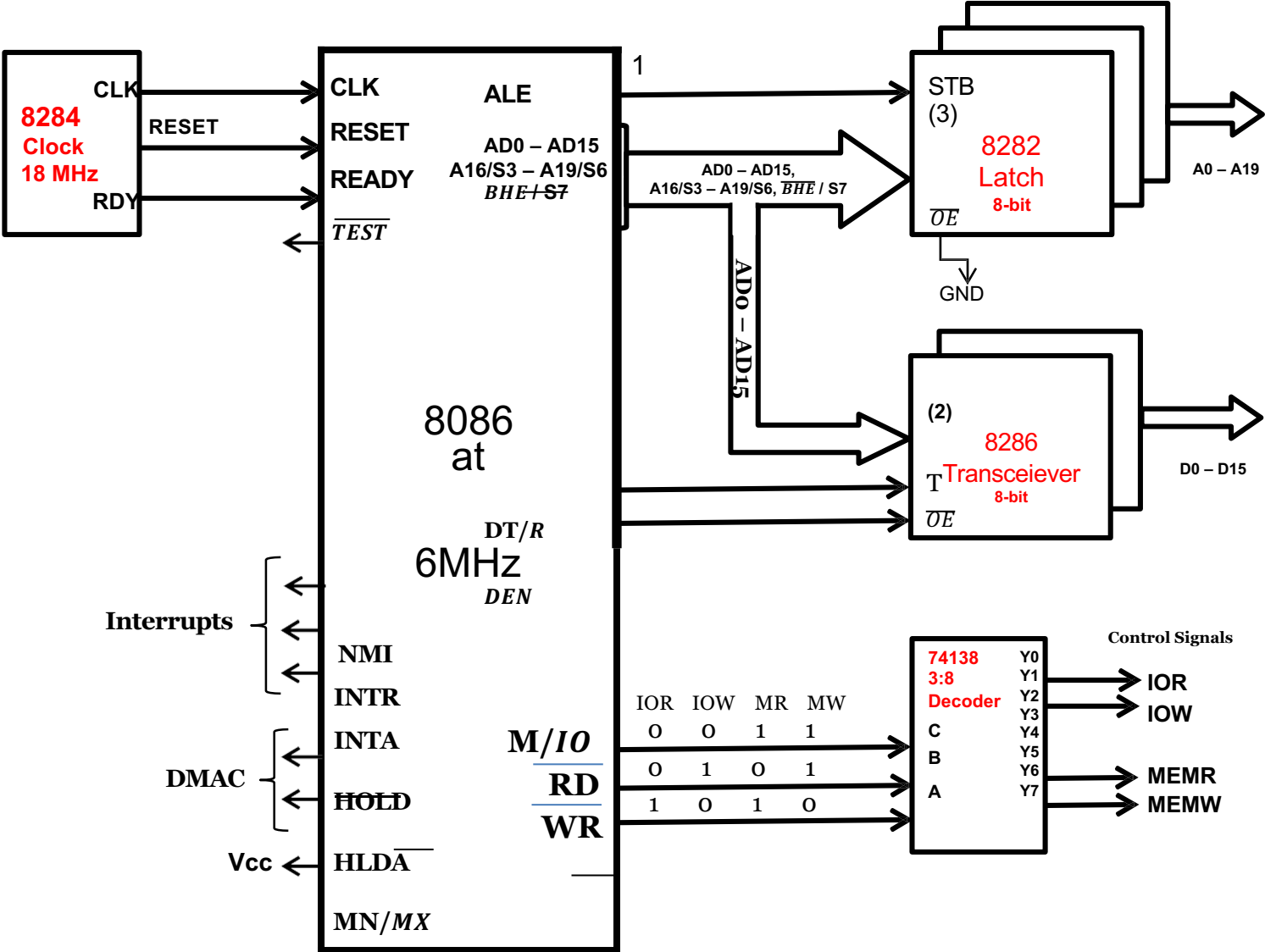








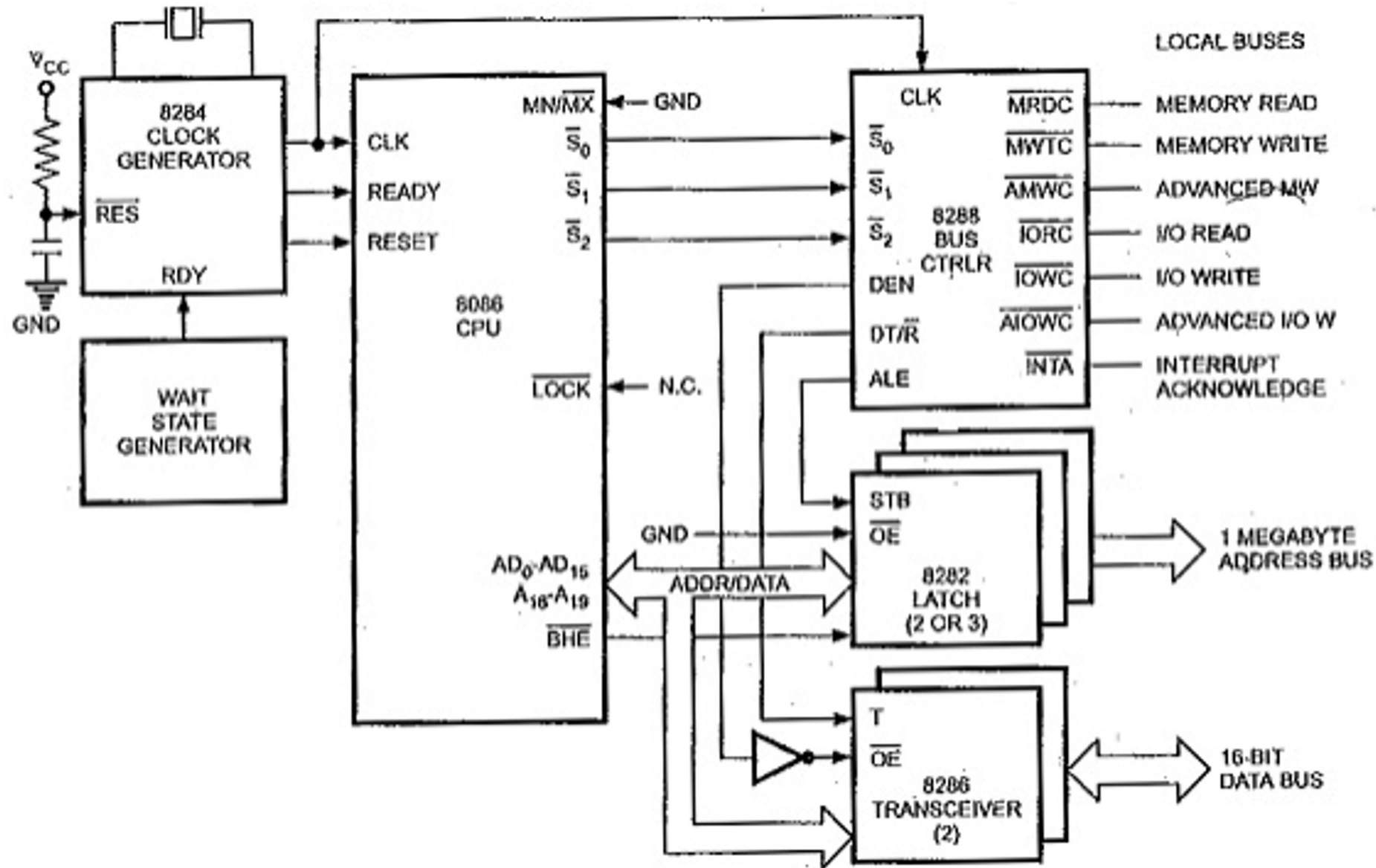
8086 in Minimum Mode!



Maximum Mode Operation

- Differs from **minimum mode** in that some control signals must be externally generated.
 - requires addition of the 8288 bus controller
- There are not enough pins on the 8086 for bus control during maximum mode
 - new pins and features replaced some of them
- **Maximum mode** used only when the system contains **external coprocessors** such as 8087.

Typical Maximum Mode Configuration



The 8288 Bus Controller

- Provides the signals eliminated from the 8086/8088 by the maximum mode operation.

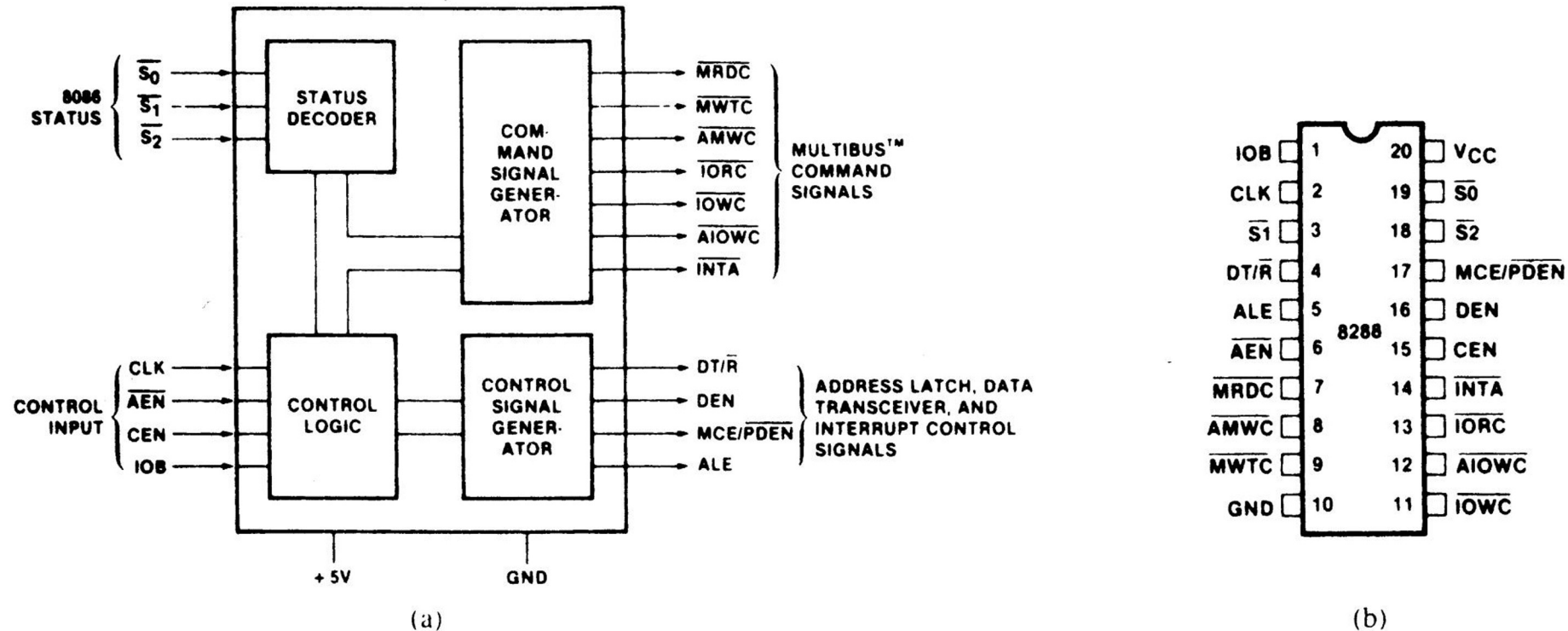


Figure 15 The 8288 bus controller; (a) block diagram and (b) pin-out.

8288 Bus Controller *Pin Functions*

S_2 , S_1 , and S_0

- **Status inputs** are connected to the status output pins on 8086/8088.
 - three signals decoded to generate timing signals

CLK

- The **clock** input provides internal timing.
 - must be connected to the CLK output pin of the 8284A clock generator

8288 Bus Controller *Pin Functions*

ALE

- The **address latch enable** output is used to demultiplex the address/data bus.

DEN

- The **data bus enable** pin controls the bidirectional data bus buffers in the system.

DT/ \bar{R}

- **Data transmit/receive** signal output to control direction of the bidirectional data bus buffers.

8288 Bus Controller *Pin Functions*

AEN

- The **address enable** input causes the 8288 to enable the memory control signals.

CEN

- The **control enable** input enables the command output pins on the 8288.

IOB

- The **I/O bus mode** input selects either I/O bus mode or system bus mode operation.

8288 Bus Controller *Pin Functions*

AIOWC

- **Advanced I/O write** is a command output to an advanced I/O write control signal.

IORC

- The **I/O read command** output provides I/O with its read control signal.

IOWC

- The **I/O write command** output provides I/O with its main write signal.

8288 *Pin Functions*

AMWT

- **Advanced memory write** control pin provides memory with an early/advanced write signal.

MWTC

- The **memory write c** control pin provides memory with its normal write control signal.

MRDC

- The **memory read c** control pin provides memory with a read control signal.

8288 Bus Controller *Pin Functions*

INTA

- The **interrupt acknowledge** output acknowledges an interrupt request input applied to the INTR pin.

MCE/PDEN

- The **master cascade/peripheral data** output selects cascade operation for an interrupt controller if IOB is grounded, and enables the I/O bus transceivers if IOB is tied high.



That's all Folks!

SUMMAR

- Both 8086 and 8088 require a single +5.0 V power supply with a **tolerance** of $\pm 10\%$.
- The 8086/8088 microprocessors are TTL-compatible if the **noise immunity** is derated to 350 mV from the customary 400 mV.
- The 8086/8088 microprocessors can drive **one** 74XX, **five** 74LSXX, **one** 74SXX, **ten** 74ALSXX, and **ten** 74HCXX unit loads.

SUMMAR

(*cont.*)

- The 8284A clock generator provides the system clock (CLK), **READY** and **RESET** synchronization.
- The standard 5 MHz 8086/8088 operating frequency is obtained by attaching a 15 MHz crystal to the 8284A clock generator.
- The PCLK output contains a TTL-**compatible** signal at one half the CLK frequency.

SUMMAR

(cont.)

- Whenever the 8086/8088 microprocessors are reset, they begin executing software at memory location FFFF0H (FFFF:0000) with the interrupt request pin disabled.
- Because the 8086/8088 buses are multiplexed and most memory and I/O devices aren't, the system must be demultiplexed before interfacing with memory or I/O.

SUMMAR

(*cont.*)

- Demultiplexing is accomplished by an 8-bit **latch** whose clock **pulse** is obtained from the **ALE** signal.
- In a large system, the buses must be buffered because the 8086/8088 microprocessors are capable of driving only **10 unit loads**, and large systems often have many more.

SUMMAR

(cont.)

- Bus timing is very important to the remaining chapters in the text. A bus cycle that consists of four clocking periods acts as the basic system timing.
- Each bus cycle is able to read or write data between the microprocessor and the memory or I/O system.

SUMMAR

(*cont.*)

- The 8086/8088 microprocessors allow the memory and I/O 460 ns to access data when they are operated with a 5 MHz clock.
- **Wait states** (T_w) stretch the bus cycle by one or more clocking periods to allow the memory and I/O additional access time.
- Wait states are **inserted** by controlling the READY input to the 8086/8088. READY is sampled at the end of T_2 and during T_w .

SUMMAR

(cont.)

- Minimum mode operation is similar to that of the Intel 8085A microprocessor, whereas maximum mode operation is new and specifically designed for the operation of the 8087 arithmetic coprocessor.
- The 8288 bus controller must be used in the maximum mode to provide the control bus signals to the memory and I/O.

SUMMAR

- This is because the maximum mode operation of the 8086/8088 removes some of the system's control signal lines in favor of control signals for the coprocessors.
- The 8288 **bus controller** reconstructs these removed control signals.

Pin Functions

The following list provides a description of each pin of the 8288 bus controller.

$S_2, S_1, \text{ and } S_0$	Status inputs are connected to the status output pins on the 8086/8088 microprocessor. These three signals are decoded to generate the timing signals for the system.
CLK	The clock input provides internal timing and must be connected to the CLK output pin of the 8284A clock generator.
ALE	The address latch enable output is used to demultiplex the address/data bus.
DEN	The data bus enable pin controls the bidirectional data bus buffers in the system. Note that this is an active high output pin that is the opposite polarity from the $\overline{\text{DEN}}$ signal found on the microprocessor when operated in the minimum mode.
DT/ $\overline{\text{R}}$	The data transmit/receive signal is output by the 8288 to control the direction of the bidirectional data bus buffers.
$\overline{\text{AEN}}$	The address enable input causes the 8288 to enable the memory control signals.
CEN	The control enable input enables the command output pins on the 8288.
IOB	The I/O bus mode input selects either the I/O bus mode or system bus mode operation.
$\overline{\text{AIOWC}}$	The advanced I/O write is a command output used to provide I/O with an advanced I/O write control signal.
$\overline{\text{IORC}}$	The I/O read command output provides I/O with its read control signal.
$\overline{\text{IOWC}}$	The I/O write command output provides I/O with its main write signal.
$\overline{\text{AMWT}}$	The advanced memory write control pin provides memory with an early or advanced write signal.
$\overline{\text{MWTC}}$	The memory write control pin provides memory with its normal write control signal.
$\overline{\text{MRDC}}$	The memory read control pin provides memory with a read control signal.
INTA	The interrupt acknowledge output acknowledges an interrupt request input applied to the INTR pin.
MCE/ $\overline{\text{PDEN}}$	The master cascade/peripheral data output selects cascade operation for an interrupt controller if IOB is grounded, and enables the I/O bus transceivers if IOB is tied high.

