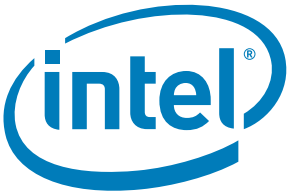
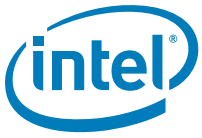


Intel® Xeon® Processor 5600 Series

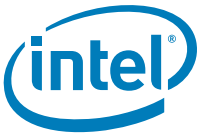
Datasheet, Volume 2

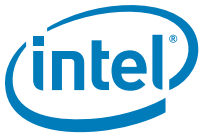
March 2010

Reference Number: 323370-001



Contents





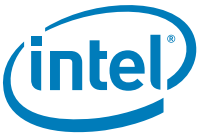
Figures

Tables

Revision History

Revision	Description	Date
-001	Initial release.	March 2010

§



1 Introduction

The Intel® Xeon® processor 5600 series is the next generation DP server/workstation processor based on the Intel® Xeon® Processor 5500 Series architecture, and utilizing 32 nm process technology. The Intel Xeon processor 5600 series upgrades Intel® 5500 platforms, and provides the following new features and capabilities:

- Up to 6-core operation (up to 12 threads per socket with Intel® Hyper-Threading Technology)
- 12 MB of shared Last-Level Cache
- Support for DDR3L (1.35 V) DIMMs
- Platform security capabilities using Intel® Trusted Execution Technology (Intel® TXT)
- Advanced Encryption Standard - New Instructions (AES-NI)
- Support for hardware-based 2X memory refresh via DDR_THERM2# pin
- Memory sparing support

This document provides Intel Xeon processor 5600 series content, and is intended to supplement the functional descriptions and register documentation found in the *Intel® Xeon® Processor 5500 Series Datasheet, Volume 2*.

1.1 References

Material and concepts available in the following documents may be beneficial when reading this document:

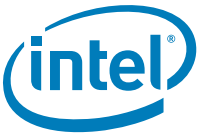
Table 1-1. References

Document	Reference #	Notes
Intel® 64 and IA-32 Architectures Software Developer's Manual • *Volume 1: Basic Architecture* • *Volume 2A: Instruction Set Reference, A-M* • *Volume 2B: Instruction Set Reference, N-Z* • *Volume 3A: System Programming Guide, Part 1* • *Volume 3B: Systems Programming Guide, Part 2*	 253665 253666 253667 253668 253669	a
Intel® 64 and IA-32 Architectures Optimization Reference Manual	248966	
Intel® Xeon® Processor 5500 Series Datasheet, Volume 2	321322	
Intel® Xeon® Processor 5600 Series Datasheet, Volume 1	323369	
Intel® Xeon® Processor 5600 Series Specification Update	323372	

Notes:

a. Document is available publicly at http://www.intel.com.

§



2 Register Description

The processor supports PCI configuration space accesses using the mechanism denoted as Configuration Mechanism in the PCI specification as defined in the *PCI Local Bus Specification*, as well as the PCI Express enhanced configuration mechanism as specified in the *PCI Express Base Specification*. All the registers are organized by bus, device, function, etc. as defined in the *PCI Express Base Specification*. All processor registers appear on the PCI bus assigned for the processor socket. Bus number is derived by the max bus range setting and processor socket number. All multi-byte numeric fields use “little-endian” ordering (that is, lower addresses contain the least significant parts of the field).

2.1 Register Terminology

Registers and register bits are assigned one or more of the following attributes. These attributes define the behavior of register and the bit(s) that are contained with in. All bits are set to default values by hard reset. Sticky bits retain their states between hard resets.

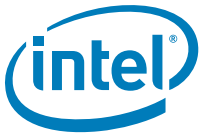
Term	Description
RO	**Read Only**. If a register bit is read only, the hardware sets its state. The bit may be read by software. Writes to this bit have no effect.
WO	**Write Only.** The register bit is not implemented as a bit. The write causes some hardware event to take place.
RW	**Read / Write**. A register bit with this attribute can be read and written by software.
RC	**Read Clear:** The bit or bits can be read by software, but the act of reading causes the value to be cleared.
RCW	**Read Clear / Write:** A register bit with this attribute will get cleared after the read. The register bit can be written.
RW1C	**Read / Write 1 Clear**. A register bit with this attribute can be read or cleared by software. In order to clear this bit, a one must be written to it. Writing a zero will have no effect.
RW0C	**Read / Write 0 Clear**. A register bit with this attribute can be read or cleared by software. In order to clear this bit, a zero must be written to it. Writing a one will have no effect.
RW1S	**Read / Write 1 Set:** A register bit can be either read or set by software. In order to set this bit, a one must be written to it. Writing a zero to this bit has no effect. Hardware will clear this bit.
RW0S	**Read / Write 0 Set:** A register bit can be either read or set by software. In order to set this bit, a zero must be written to it. Writing a one to this bit has no effect. Hardware will clear this bit.
RWL	**Read / Write / Lock**. A register bit with this attribute can be read or written by software. Hardware or a configuration bit can lock the bit and prevent it from being updated.
RWO	**Read / Write Once.** A register bit with this attribute can be written to only once after power up. After the first write, the bit becomes read only. This attribute is applied on a bit by bit basis. For example, if the RWO attribute is applied to a 2 bit field, and only one bit is written, then the written bit cannot be rewritten (unless reset). The unwritten bit, of the field, may still be written once. This is special case of RWL.
RRW	**Read / Restricted Write.** This bit can be read and written by software. However, only supported values will be written. Writes of non supported values will have no effect.
L	**Lock.** A register bit with this attribute becomes Read Only after a lock bit is set.
RSVD	**Reserved Bit.** This bit is reserved for future expansion and must not be written. The *PCI Local Bus Specification,* Revision 2.2 requires that reserved bits must be preserved. Any software that modifies a register that contains a reserved bit is responsible for reading the register, modifying the desired bits, and writing back the result.

Term	Description
Reserved Bits	Some of the processor registers described in this section contain reserved bits. These bits are labeled “Reserved”. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note that software does not need to perform a read-merge-write operation for the Configuration Address (CONFIG_ADDRESS) register.
Reserved Registers	In addition to reserved bits within a register, the processor contains address locations in the configuration space that are marked either “Reserved” or “Intel Reserved”. The processor responds to accesses to “Reserved” address locations by completing the host cycle. When a “Reserved” register location is read, a zero value is returned. (“Reserved” registers can be 8, 16, or 32 bits in size). Writes to “Reserved” registers have no effect on the processor. Registers that are marked as “Intel Reserved” must not be modified by system software. Writes to “Intel Reserved” registers may cause system failure. Reads to “Intel Reserved” registers may return a non-zero value.
Default Value upon a Reset	Upon a reset, the processor sets all of its internal configuration registers to predetermined default states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the processor registers accordingly.
“ST” appended to the end of a bit name	The bit is “sticky” or unchanged by a hard reset. These bits can only be cleared by a PWRGOOD reset.

2.2 Platform Configuration Structure

The processor contains 6 PCI devices within a single physical component. The configuration registers for these devices are mapped as devices residing on the PCI bus assigned for the processor socket. Bus number is derived by the max bus range setting and processor socket number.

- **Device 0:** Generic processor non-core. Device 0, Function 0 contains the generic non-core configuration registers for the processor and resides at DID (Device ID) of 2C70h. Device 0, Function 1 contains the System Address Decode registers and resides at DID of 2D81h.
- **Device 2:** Intel® QuickPath Interconnect (Intel® QPI). Device 2, Function 0 contains the Intel QuickPath Interconnect configuration registers for Intel QPI Link 0 and resides at DID of 2D90h. Device 2, Function 1 contains the physical layer registers for Intel QPI Link 0 and resides at DID of 2D91h. Device 2, Function 2 contains the mirror port registers for Intel QPI Link 0 and resides at DID of 2D92h. Device 2, Function 3 contains the mirror port registers for Intel QPI Link 1 and resides at DID of 2D93h. Device 2, Function 4 contains the Intel QuickPath configuration registers for Intel® QuickPath Interconnect Link 1 and resides at DID of 2D94h. Device 2, Function 5 contains the physical layer registers for Intel QPI Link 1 and resides at DID of 2D95h. Functions 4 and 5 only apply to processors with two Intel QPI links.
- **Device 3:** Integrated Memory Controller. Device 3, Function 0 contains the general registers for the Integrated Memory Controller and resides at DID of 2D98h. Device 3, Function 1 contains the Target Address Decode registers for the Integrated Memory Controller and resides at DID of 2D99h. Device 3, Function 2 contains the RAS registers for the Integrated Memory Controller and resides at DID of 2D9Ah. Device 3, Function 4 contains the test registers for the Integrated Memory Controller and resides at DID of 2D9Ch. Function 2 only applies to processors supporting registered DIMMs.
- **Device 4:** Integrated Memory Controller Channel 0. Device 4, Function 0 contains the control registers for Integrated Memory Controller Channel 0 and resides at



DID of 2DA0h. Device 4, Function 1 contains the address registers for Integrated Memory Controller Channel 0 and resides at DID of 2DA1h. Device 4, Function 2 contains the rank registers for Integrated Memory Controller Channel 0 and resides at DID of 2DA2h. Device 4, Function 3 contains the thermal control registers for Integrated Memory Controller Channel 0 and resides at DID of 2DA3h.

- **Device 5:** Integrated Memory Controller Channel 1. Device 5, Function 0 contains the control registers for Integrated Memory Controller Channel 1 and resides at DID of 2DA8h. Device 5, Function 1 contains the address registers for Integrated Memory Controller Channel 1 and resides at DID of 2DA9h. Device 5, Function 2 contains the rank registers for Integrated Memory Controller Channel 1 and resides at DID of 2DAAh. Device 5, Function 3 contains the thermal control registers for Integrated Memory Controller Channel 1 and resides at DID of 2DABh.
- **Device 6:** Integrated Memory Controller Channel 2. Device 6, Function 0 contains the control registers for Integrated Memory Controller Channel 2 and resides at DID of 2DB0h. Device 6, Function 1 contains the address registers for Integrated Memory Controller Channel 2 and resides at DID of 2DB1h. Device 6, Function 2 contains the rank registers for Integrated Memory Controller Channel 2 and resides at DID of 2DB2h. Device 6, Function 3 contains the thermal control registers for Integrated Memory Controller Channel 2 and resides at DID of 2DB3h.

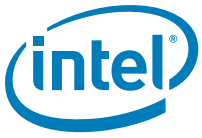
2.3 Device Mapping

Each component in the processor is uniquely identified by a PCI bus address consisting of Bus Number, Device Number and Function Number. Device configuration is based on the PCI Type 0 configuration conventions. All processor registers appear on the PCI bus assigned for the processor socket. Bus number is derived by the max bus range setting and processor socket number.

Table 2-1. Functions Specifically Handled by the Processor

Component	Register Group	DID	Device	Function
Processor	Intel® QuickPath Architecture Generic Non-core Registers	2C70h	0	0
	Intel® QuickPath Architecture System Address Decoder	2D81h		1
	Intel® QuickPath Interconnect (Intel® QPI) Link 0	2D90h	2	0
	Intel QPI Physical 0	2D91h		1
	Mirror Port Link 0	2D92h		2
	Mirror Port Link 1	2D93h		3
	Intel QPI Link 1	2D94h		4[1]
	Intel QPI Physical 1	2D95h		5[1]
	Integrated Memory Controller Registers	2D98h	3	0
	Integrated Memory Controller Target Address Decoder	2D99h		1
	Integrated Memory Controller RAS Registers	2D9Ah		2[2]
	Integrated Memory Controller Test Registers	2D9Ch		4
	Integrated Memory Controller Channel 0 Control	2DA0h	4	0
	Integrated Memory Controller Channel 0 Address	2DA1h		1
	Integrated Memory Controller Channel 0 Rank	2DA2h		2
	Integrated Memory Controller Channel 0 Thermal Control	2DA3h		3
	Integrated Memory Controller Channel 1 Control	2DA8h	5	0
	Integrated Memory Controller Channel 1 Address	2DA9h		1
	Integrated Memory Controller Channel 1 Rank	2DAAh		2
	Integrated Memory Controller Channel 1 Thermal Control	2DABh		3
	Integrated Memory Controller Channel 2 Control	2DB0h	6	0
	Integrated Memory Controller Channel 2 Address	2DB1h		1
	Integrated Memory Controller Channel 2 Rank	2DB2h		2
	Integrated Memory Controller Channel 2 Thermal Control	2DB3h		3

Notes:
1. Applies only to processors with two Intel QPI links.
2. Applies only to processors supporting sparing, mirroring and scrubbing RAS features.



2.4 Detailed Configuration Space Maps

Table 2-2. Device 0, Function 0: Generic Non-core Registers

DID	VID	00h	DESIRED_CORES		80h
PCISTS	PCICMD	04h			84h
CCR	RID	08h	MEMLOCK_STATUS		88h
HDR		0Ch			8Ch
		10h	MC_CFG_CONTROL		90h
		14h			94h
		18h			98h
		1Ch			9Ch
		20h			A0h
		24h			A4h
		28h			A8h
SID	SVID	2Ch			ACh
		30h	POWER_CNTRL_ERR_STATUS		B0h
		34h			B4h
		38h			B8h
		3Ch			BCh
MAXREQUEST_LC		40h	CURRENT_UCLK_RATIO		C0h
MAXREQUEST_LS		44h			C4h
MAXREQUEST_LL		48h			C8h
		4Ch			CCh
		50h	MIRROR_PORT_CTL		D0h
		54h			D4h
		58h			D8h
		5Ch			DCh
MAX_RTIDS		60h			E0h
		64h			E4h
		68h			E8h
		6Ch			ECh
		70h			F0h
		74h			F4h
		78h			F8h
		7Ch			FCh

Table 2-3. Device 0, Function 1: System Address Decoder Registers

DID	VID	00h	SAD_DRAM_RULE_0	80h
PCISTS	PCICMD	04h	SAD_DRAM_RULE_1	84h
CCR	RID	08h	SAD_DRAM_RULE_2	88h
HDR		0Ch	SAD_DRAM_RULE_3	8Ch
		10h	SAD_DRAM_RULE_4	90h
		14h	SAD_DRAM_RULE_5	94h
		18h	SAD_DRAM_RULE_6	98h
		1Ch	SAD_DRAM_RULE_7	9Ch
		20h		A0h
		24h		A4h
		28h		A8h
SID	SVID	2Ch		ACh
		30h		B0h
		34h		B4h
		38h		B8h
		3Ch		BCh
SAD_PAM0123		40h	SAD_INTERLEAVE_LIST_0	C0h
SAD_PAM456		44h	SAD_INTERLEAVE_LIST_1	C4h
SAD_HEN		48h	SAD_INTERLEAVE_LIST_2	C8h
SAD_SMRAM		4Ch	SAD_INTERLEAVE_LIST_3	CCh
SAD_PCIEXBAR		50h	SAD_INTERLEAVE_LIST_4	D0h
		54h	SAD_INTERLEAVE_LIST_5	D4h
		58h	SAD_INTERLEAVE_LIST_6	D8h
		5Ch	SAD_INTERLEAVE_LIST_7	DCh
SAD_MCSEG_BASE		60h		E0h
		64h		E4h
SAD_MCSEG_MASK		68h		E8h
		6Ch		ECh
SAD_MESEG_BASE		70h		F0h
		74h		F4h
SAD_MESEG_MASK		78h		F8h
		7Ch		FCh

Table 2-4. Device 2, Function 0: Intel QPI Link 0 Registers

DID	VID	00h			80h
PCISTS	PCICMD	04h			84h
CCR	RID	08h			88h
HDR		0Ch			8Ch
		10h			90h
		14h			94h
		18h			98h
		1Ch			9Ch
		20h			A0h
		24h			A4h
		28h			A8h
SID	SVID	2Ch			ACh
		30h			B0h
		34h			B4h
		38h			B8h
		3Ch			BCh
QPI_QPILCP_L0		40h	QPI_RMT_QPILP0_STAT_L0		C0h
		44h	QPI_RMT_QPILP1_STAT_L0		C4h
QPI_QPILCL_L0		48h	QPI_RMT_QPILP2_STAT_L0		C8h
		4Ch	QPI_RMT_QPILP3_STAT_L0		CCh
QPI_QPILS_L0		50h			D0h
		54h			D4h
QPI_DEF_RMT_VN_CREDITS_L0		58h			D8h
		5Ch			DCh
		60h			E0h
		64h			E4h
		68h			E8h
		6Ch			ECh
		70h			F0h
		74h			F4h
		78h			F8h
		7Ch			FCh

Table 2-5. Device 2, Function 1: Intel QPI Physical 0 Registers

DID	VID	00h	QPI_0_PH_PIS	80h	
PCISTS	PCICMD	04h		84h	
CCR	RID	08h		88h	
HDR		0Ch		8Ch	
		10h		90h	
		14h	QPI_0_PH_PTV	94h	
		18h		98h	
		1Ch	QPI_0_PH_LDC	9Ch	
		20h		A0h	
		24h	QPI_0_PH_PRT	A4h	
		28h		A8h	
SID	SVID	2Ch		ACh	
		30h		B0h	
		34h		B4h	
		38h		B8h	
		3Ch		BCh	
		40h		C0h	
		44h		C4h	
		48h		C8h	
		4Ch		CCh	
QPI_0_PLL_STATUS		50h	QPI_0_PH_PMR0	D0h	
QPI_0_PLL_RATIO		54h		D4h	
		58h		D8h	
		5Ch		DCh	
		60h	QPI_0_EP_SR	E0h	
		64h		E4h	
QPI_0_PH_CPR		68h		E8h	
QPI_0_PH_CTR		6Ch		ECh	
		70h		F0h	
		74h	QPI_0_EP_MCTR	F4h	
		78h		F8h	
		7Ch		FCh	

Table 2-6. Device 2, Function 2: Mirror Port Link 0 Registers

DID	VID	00h			80h
PCISTS	PCICMD	04h			84h
CCR	RID	08h			88h
HDR		0Ch			8Ch
		10h			90h
		14h			94h
		18h			98h
		1Ch			9Ch
		20h			A0h
		24h	MIP_PH_PRT_L0		A4h
		28h			A8h
SID	SVID	2Ch			ACh
		30h			B0h
		34h			B4h
		38h			B8h
		3Ch			BCh
		40h			C0h
		44h			C4h
		48h			C8h
		4Ch			CCh
		50h			D0h
		54h			D4h
		58h			D8h
		5Ch			DCh
		60h			E0h
		64h			E4h
		68h			E8h
MIP_PH_CTR_L0		6Ch			ECh
		70h			F0h
		74h			F4h
		78h			F8h
		7Ch			FCh

Table 2-7. Device 2, Function 3: Mirror Port Link 1 Registers

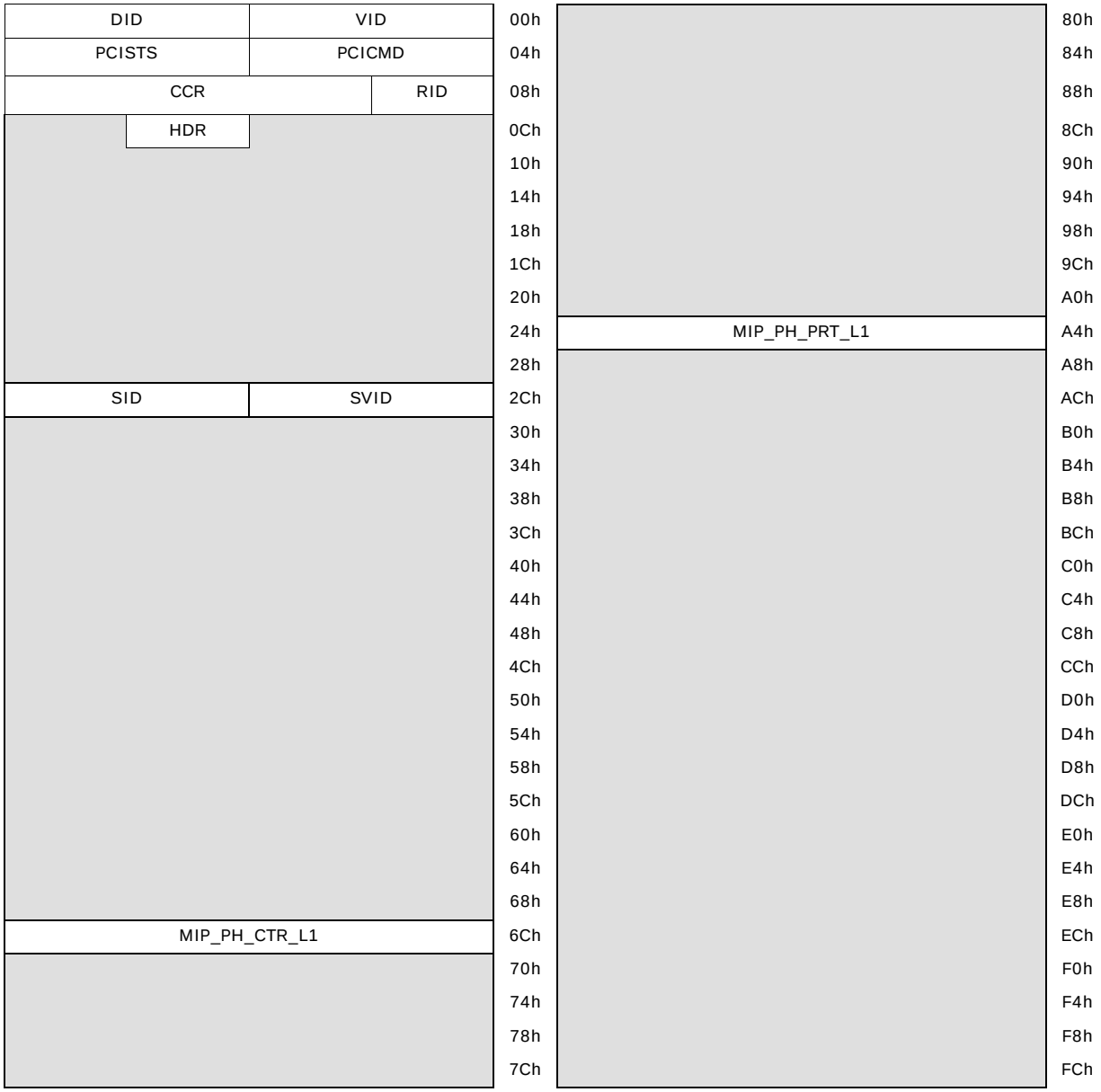


Table 2-8. Device 2, Function 4: Intel QPI Link 1 Registers[1]

DID	VID	00h			80h
PCISTS	PCICMD	04h			84h
CCR	RID	08h			88h
BIST	HDR	0Ch			8Ch
		10h			90h
		14h			94h
		18h			98h
		1Ch			9Ch
		20h			A0h
		24h			A4h
		28h			A8h
SID	SVID	2Ch			ACh
		30h			B0h
		34h			B4h
		38h			B8h
		3Ch			BCh
QPI_QPILCP_L1		40h	QPI_RMT_QPILP0_STAT_L1		C0h
		44h	QPI_RMT_QPILP1_STAT_L1		C4h
QPI_QPILCL_L1		48h	QPI_RMT_QPILP2_STAT_L1		C8h
		4Ch	QPI_RMT_QPILP3_STAT_L1		CCh
QPI_QPILS_L1		50h			D0h
		54h			D4h
QPI_DEF_RMT_VN_CREDITS_L1		58h			D8h
		5Ch			DCh
		60h			E0h
		64h			E4h
		68h			E8h
		6Ch			ECh
		70h			F0h
		74h			F4h
		78h			F8h
		7Ch			FCh

Note:
1. Applies only to processors with two Intel QPI links.

Table 2-9. Device 2, Function 5: Intel QPI Physical 1 Registers

DID	VID	00h	QPI_1_PH_PIS	80h	
PCISTS	PCICMD	04h		84h	
CCR	RID	08h		88h	
HDR		0Ch		8Ch	
		10h		90h	
		14h	QPI_1_PH_PTV	94h	
		18h		98h	
		1Ch	QPI_1_PH_LDC	9Ch	
		20h		A0h	
		24h	QPI_1_PH_PRT	A4h	
		28h		A8h	
SID	SVID	2Ch		ACh	
		30h		B0h	
		34h		B4h	
		38h		B8h	
		3Ch		BCh	
		40h		C0h	
		44h		C4h	
		48h		C8h	
		4Ch		CCh	
QPI_1_PLL_STATUS		50h	QPI_1_PH_PMR0	D0h	
QPI_1_PLL_RATIO		54h		D4h	
		58h		D8h	
		5Ch		DCh	
		60h	QPI_1_EP_SR	E0h	
		64h		E4h	
QPI_1_PH_CPR		68h		E8h	
QPI_1_PH_CTR		6Ch		ECh	
		70h		F0h	
		74h	QPI_1_EP_MCTR	F4h	
		78h		F8h	
		7Ch		FCh	

Table 2-10. Device 3, Function 0: Integrated Memory Controller Registers

DID	VID	00h
PCISTS	PCICMD	04h
CCR	RID	08h
HDR		0Ch
		10h
		14h
		18h
		1Ch
		20h
		24h
		28h
SID	SVID	2Ch
		30h
		34h
		38h
		3Ch
		40h
		44h
MC_CONTROL		48h
MC_STATUS		4Ch
MC_SMI_DIMM_ERROR_STATUS		50h
MC_SMI_CNTRL		54h
		58h
MC_RESET_CONTROL		5Ch
MC_CHANNEL_MAPPER		60h
MC_MAX_DOD		64h
		68h
		6Ch
MC_RD_CRDT_INIT		70h
MC_CRDT_WR_THLD		74h
MC_SCRUBADDR_LO		78h
MC_SCRUBADDR_HI		7Ch

	80h
	84h
	88h
	8Ch
	90h
	94h
	98h
	9Ch
	A0h
	A4h
	A8h
	ACh
	B0h
	B4h
	B8h
	BCh
	C0h
	C4h
	C8h
	CCh
	D0h
	D4h
	D8h
	DCh
	E0h
	E4h
	E8h
	ECh
	F0h
	F4h
	F8h
	FCh

Table 2-11. Device 3, Function 1: Target Address Decoder Registers

DID	VID	00h	TAD_DRAM_RULE_0	80h	
PCISTS	PCICMD	04h	TAD_DRAM_RULE_1	84h	
CCR	RID	08h	TAD_DRAM_RULE_2	88h	
HDR		0Ch	TAD_DRAM_RULE_3	8Ch	
		10h	TAD_DRAM_RULE_4	90h	
		14h	TAD_DRAM_RULE_5	94h	
		18h	TAD_DRAM_RULE_6	98h	
		1Ch	TAD_DRAM_RULE_7	9Ch	
		20h		A0h	
		24h		A4h	
		28h		A8h	
SID	SVID	2Ch		ACh	
		30h		B0h	
		34h		B4h	
		38h		B8h	
		3Ch		BCh	
		40h	TAD_INTERLEAVE_LIST_0	C0h	
		44h	TAD_INTERLEAVE_LIST_1	C4h	
		48h	TAD_INTERLEAVE_LIST_2	C8h	
		4Ch	TAD_INTERLEAVE_LIST_3	CCh	
		50h	TAD_INTERLEAVE_LIST_4	D0h	
		54h	TAD_INTERLEAVE_LIST_5	D4h	
		58h	TAD_INTERLEAVE_LIST_6	D8h	
		5Ch	TAD_INTERLEAVE_LIST_7	DCh	
		60h		E0h	
		64h		E4h	
		68h		E8h	
		6Ch		ECh	
		70h		F0h	
		74h		F4h	
		78h		F8h	
		7Ch		FCh	

Table 2-12. Device 3, Function 2: Integrated Memory Controller RAS Registers[1]

DID	VID	00h	MC_COR_ECC_CNT_0	80h
PCISTS	PCICMD	04h	MC_COR_ECC_CNT_1	84h
CCR	RID	08h	MC_COR_ECC_CNT_2	88h
HDR		0Ch	MC_COR_ECC_CNT_3	8Ch
		10h	MC_COR_ECC_CNT_4	90h
		14h	MC_COR_ECC_CNT_5	94h
		18h		98h
		1Ch		9Ch
		20h		A0h
		24h		A4h
		28h		A8h
SID	SVID	2Ch		ACh
		30h		B0h
		34h		B4h
		38h		B8h
		3Ch		BCh
		40h		C0h
		44h		C4h
MC_SSRCONTROL		48h		C8h
MC_SCRUB_CONTROL		4Ch		CCh
MC_RAS_ENABLES		50h		D0h
MC_RAS_STATUS		54h		D4h
		58h		D8h
		5Ch		DCh
MC_SSRSTATUS		60h		E0h
		64h		E4h
		68h		E8h
		6Ch		ECh
		70h		F0h
		74h		F4h
		78h		F8h
		7Ch		FCh

Note:
1. Applies only to processors supporting registered DIMMs.

Table 2-13. Device 3, Function 4: Integrated Memory Controller Test Registers

DID	VID	00h	MC_TEST_PH_PIS	80h	
PCISTS	PCICMD	04h		84h	
CCR	RID	08h		88h	
HDR		0Ch		8Ch	
		10h		90h	
		14h		94h	
		18h		98h	
		1Ch		9Ch	
		20h		A0h	
		24h		A4h	
		28h	MC_TEST_PAT_GCTR	A8h	
SID	SVID	2Ch		ACh	
		30h	MC_TEST_PAT_BA	B0h	
		34h		B4h	
		38h		B8h	
		3Ch	MC_TEST_PAT_IS	BCh	
		40h	MC_TEST_PAT_DCD	C0h	
		44h		C4h	
		48h		C8h	
		4Ch		CCh	
MC_DIMM_CLK_RATIO_STATUS		50h		D0h	
MC_DIMM_CLK_RATIO		54h		D4h	
		58h		D8h	
		5Ch		DCh	
MC_TEST_ERR_RCV1		60h		E0h	
MC_TEST_ERR_RCV0		64h		E4h	
		68h		E8h	
MC_TEST_PH_CTR		6Ch		ECh	
		70h		F0h	
		74h		F4h	
		78h		F8h	
		7Ch		FCh	

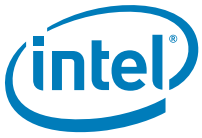


Table 2-14. Device 4, Function 0: Integrated Memory Controller Channel 0 Control Registers

DID	VID	00h	MC_CHANNEL_0_RANK_TIMING_A	80h
PCISTS	PCICMD	04h	MC_CHANNEL_0_RANK_TIMING_B	84h
CCR	RID	08h	MC_CHANNEL_0_BANK_TIMING	88h
HDR		0Ch	MC_CHANNEL_0_REFRESH_TIMING	8Ch
		10h	MC_CHANNEL_0_CKE_TIMING	90h
		14h	MC_CHANNEL_0_ZQ_TIMING	94h
		18h	MC_CHANNEL_0_RCOMP_PARAMS	98h
		1Ch	MC_CHANNEL_0_ODT_PARAMS1	9Ch
		20h	MC_CHANNEL_0_ODT_PARAMS2	A0h
		24h	MC_CHANNEL_0_ODT_MATRIX_RANK_0_3_RD	A4h
		28h	MC_CHANNEL_0_ODT_MATRIX_RANK_4_7_RD	A8h
SID	SVID	2Ch	MC_CHANNEL_0_ODT_MATRIX_RANK_0_3_WR	ACh
		30h	MC_CHANNEL_0_ODT_MATRIX_RANK_4_7_WR	B0h
		34h	MC_CHANNEL_0_WAQ_PARAMS	B4h
		38h	MC_CHANNEL_0_SCHEDULER_PARAMS	B8h
		3Ch	MC_CHANNEL_0_MAINTENANCE_OPS	BCh
		40h	MC_CHANNEL_0_TX_BG_SETTINGS	C0h
		44h		C4h
		48h	MC_CHANNEL_0_RX_BGF_SETTINGS	C8h
		4Ch	MC_CHANNEL_0_EW_BGF_SETTINGS	CCh
MC_CHANNEL_0_DIMM_RESET_CMD		50h	MC_CHANNEL_0_EW_BGF_OFFSET_SETTINGS	D0h
MC_CHANNEL_0_DIMM_INIT_CMD		54h	MC_CHANNEL_0_ROUND_TRIP_LATENCY	D4h
MC_CHANNEL_0_DIMM_INIT_PARAMS		58h	MC_CHANNEL_0_PAGETABLE_PARAMS1	D8h
MC_CHANNEL_0_DIMM_INIT_STATUS		5Ch	MC_CHANNEL_0_PAGETABLE_PARAMS2	DCh
MC_CHANNEL_0_DDR3CMD		60h	MC_TX_BG_CMD_DATA_RATIO_SETTING_CH0	E0h
		64h	MC_TX_BG_CMD_OFFSET_SETTINGS_CH0	E4h
MC_CHANNEL_0_REFRESH_THROTTLE_SUPPORT		68h	MC_TX_BG_DATA_OFFSET_SETTINGS_CH0	E8h
		6Ch		ECh
MC_CHANNEL_0_MRS_VALUE_0_1		70h	MC_CHANNEL_0_ADDR_MATCH	F0h
MC_CHANNEL_0_MRS_VALUE_2		74h		F4h
MC_CHANNEL_0_CKE_TIMING_B		78h	MC_CHANNEL_0_ECC_ERROR_MASK	F8h
MC_CHANNEL_0_RANK_PRESENT		7Ch	MC_CHANNEL_0_ECC_ERROR_INJECT	FCh

Table 2-15. Device 4, Function 1: Integrated Memory Controller Channel 0 Address Registers

DID	VID	00h
PCISTS	PCICMD	04h
CCR	RID	08h
HDR		0Ch
		10h
		14h
		18h
		1Ch
		20h
		24h
		28h
SID	SVID	2Ch
		30h
		34h
		38h
		3Ch
		40h
		44h
MC_DOD_CH0_0		48h
MC_DOD_CH0_1		4Ch
MC_DOD_CH0_2		50h
		54h
		58h
		5Ch
		60h
		64h
		68h
		6Ch
		70h
		74h
		78h
		7Ch

MC_SAG_CH0_0	80h
MC_SAG_CH0_1	84h
MC_SAG_CH0_2	88h
MC_SAG_CH0_3	8Ch
MC_SAG_CH0_4	90h
MC_SAG_CH0_5	94h
MC_SAG_CH0_6	98h
MC_SAG_CH0_7	9Ch
	A0h
	A4h
	A8h
	ACh
	B0h
	B4h
	B8h
	BCh
	C0h
	C4h
	C8h
	CCh
	D0h
	D4h
	D8h
	DCh
	E0h
	E4h
	E8h
	ECh
	F0h
	F4h
	F8h
	FCh

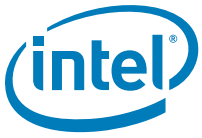


Table 2-16. Device 4, Function 2: Integrated Memory Controller Channel 0 Rank Registers

DID	VID	00h	MC_RIR_WAY_CH0_0	80h
PCISTS	PCICMD	04h	MC_RIR_WAY_CH0_1	84h
CCR	RID	08h	MC_RIR_WAY_CH0_2	88h
HDR		0Ch	MC_RIR_WAY_CH0_3	8Ch
		10h	MC_RIR_WAY_CH0_4	90h
		14h	MC_RIR_WAY_CH0_5	94h
		18h	MC_RIR_WAY_CH0_6	98h
		1Ch	MC_RIR_WAY_CH0_7	9Ch
		20h	MC_RIR_WAY_CH0_8	A0h
		24h	MC_RIR_WAY_CH0_9	A4h
		28h	MC_RIR_WAY_CH0_10	A8h
SID	SVID	2Ch	MC_RIR_WAY_CH0_11	ACh
		30h	MC_RIR_WAY_CH0_12	B0h
		34h	MC_RIR_WAY_CH0_13	B4h
		38h	MC_RIR_WAY_CH0_14	B8h
		3Ch	MC_RIR_WAY_CH0_15	BCh
MC_RIR_LIMIT_CH0_0		40h	MC_RIR_WAY_CH0_16	C0h
MC_RIR_LIMIT_CH0_1		44h	MC_RIR_WAY_CH0_17	C4h
MC_RIR_LIMIT_CH0_2		48h	MC_RIR_WAY_CH0_18	C8h
MC_RIR_LIMIT_CH0_3		4Ch	MC_RIR_WAY_CH0_19	CCh
MC_RIR_LIMIT_CH0_4		50h	MC_RIR_WAY_CH0_20	D0h
MC_RIR_LIMIT_CH0_5		54h	MC_RIR_WAY_CH0_21	D4h
MC_RIR_LIMIT_CH0_6		58h	MC_RIR_WAY_CH0_22	D8h
MC_RIR_LIMIT_CH0_7		5Ch	MC_RIR_WAY_CH0_23	DCh
		60h	MC_RIR_WAY_CH0_24	E0h
		64h	MC_RIR_WAY_CH0_25	E4h
		68h	MC_RIR_WAY_CH0_26	E8h
		6Ch	MC_RIR_WAY_CH0_27	ECh
		70h	MC_RIR_WAY_CH0_28	F0h
		74h	MC_RIR_WAY_CH0_29	F4h
		78h	MC_RIR_WAY_CH0_30	F8h
		7Ch	MC_RIR_WAY_CH0_31	FCh

Table 2-17. Device 4, Function 3: Integrated Memory Controller Channel 0 Thermal Control Registers

DID	VID	00h	MC_COOLING_COEF0	80h
PCISTS	PCICMD	04h	MC_CLOSED_LOOP0	84h
CCR	RID	08h	MC_THROTTLE_OFFSET0	88h
HDR		0Ch		8Ch
		10h		90h
		14h		94h
		18h	MC_RANK_VIRTUAL_TEMP0	98h
		1Ch	MC_DDR_THERM0_COMMAND0	9Ch
		20h	MC_DDR_THERM1_COMMAND0	A0h
		24h	MC_DDR_THERM0_STATUS0	A4h
		28h	MC_DDR_THERM1_STATUS0	A8h
SID	SVID	2Ch		ACh
		30h		B0h
		34h		B4h
		38h		B8h
		3Ch		BCh
		40h		C0h
		44h		C4h
MC_THERMAL_CONTROL0		48h		C8h
MC_THERMAL_STATUS0		4Ch		CCh
MC_THERMAL_DEFEATURE0		50h		D0h
		54h		D4h
		58h		D8h
		5Ch		DCh
MC_THERMAL_PARAMS_A0		60h		E0h
MC_THERMAL_PARAMS_B0		64h		E4h
		68h		E8h
		6Ch		ECh
		70h		F0h
		74h		F4h
		78h		F8h
		7Ch		FCh

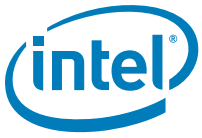


Table 2-18. Device 5, Function 0: Integrated Memory Controller Channel 1 Control Registers

DID	VID	00h	MC_CHANNEL_1_RANK_TIMING_A	80h
PCISTS	PCICMD	04h	MC_CHANNEL_1_RANK_TIMING_B	84h
CCR	RID	08h	MC_CHANNEL_1_BANK_TIMING	88h
HDR		0Ch	MC_CHANNEL_1_REFRESH_TIMING	8Ch
		10h	MC_CHANNEL_1_CKE_TIMING	90h
		14h	MC_CHANNEL_1_ZQ_TIMING	94h
		18h	MC_CHANNEL_1_RCOMP_PARAMS	98h
		1Ch	MC_CHANNEL_1_ODT_PARAMS1	9Ch
		20h	MC_CHANNEL_1_ODT_PARAMS2	A0h
		24h	MC_CHANNEL_1_ODT_MATRIX_RANK_0_3_RD	A4h
		28h	MC_CHANNEL_1_ODT_MATRIX_RANK_4_7_RD	A8h
SID	SVID	2Ch	MC_CHANNEL_1_ODT_MATRIX_RANK_0_3_WR	ACh
		30h	MC_CHANNEL_1_ODT_MATRIX_RANK_4_7_WR	B0h
		34h	MC_CHANNEL_1_WAQ_PARAMS	B4h
		38h	MC_CHANNEL_1_SCHEDULER_PARAMS	B8h
		3Ch	MC_CHANNEL_1_MAINTENANCE_OPS	BCh
		40h	MC_CHANNEL_1_TX_BG_SETTINGS	C0h
		44h		C4h
		48h	MC_CHANNEL_1_RX_BGF_SETTINGS	C8h
		4Ch	MC_CHANNEL_1_EW_BGF_SETTINGS	CCh
MC_CHANNEL_1_DIMM_RESET_CMD		50h	MC_CHANNEL_1_EW_BGF_OFFSET_SETTINGS	D0h
MC_CHANNEL_1_DIMM_INIT_CMD		54h	MC_CHANNEL_1_ROUND_TRIP_LATENCY	D4h
MC_CHANNEL_1_DIMM_INIT_PARAMS		58h	MC_CHANNEL_1_PAGETABLE_PARAMS1	D8h
MC_CHANNEL_1_DIMM_INIT_STATUS		5Ch	MC_CHANNEL_1_PAGETABLE_PARAMS2	DCh
MC_CHANNEL_1_DDR3CMD		60h	MC_TX_BG_CMD_DATA_RATIO_SETTING_CH1	E0h
		64h	MC_TX_BG_CMD_OFFSET_SETTINGS_CH1	E4h
MC_CHANNEL_1_REFRESH_THROTTLE_SUPPORT		68h	MC_TX_BG_DATA_OFFSET_SETTINGS_CH1	E8h
		6Ch		ECh
MC_CHANNEL_1_MRS_VALUE_0_1		70h	MC_CHANNEL_1_ADDR_MATCH	F0h
MC_CHANNEL_1_MRS_VALUE_2		74h		F4h
MC_CHANNEL_1_CKE_TIMING_B		78h	MC_CHANNEL_1_ECC_ERROR_MASK	F8h
MC_CHANNEL_1_RANK_PRESENT		7Ch	MC_CHANNEL_1_ECC_ERROR_INJECT	FCh

Table 2-19. Device 5, Function 1: Integrated Memory Controller Channel 1 Address Registers

DID	VID	00h
PCISTS	PCICMD	04h
CCR	RID	08h
HDR		0Ch
		10h
		14h
		18h
		1Ch
		20h
		24h
		28h
SID	SVID	2Ch
		30h
		34h
		38h
		3Ch
		40h
		44h
MC_DOD_CH1_0		48h
MC_DOD_CH1_1		4Ch
MC_DOD_CH1_2		50h
		54h
		58h
		5Ch
		60h
		64h
		68h
		6Ch
		70h
		74h
		78h
		7Ch

MC_SAG_CH1_0	80h
MC_SAG_CH1_1	84h
MC_SAG_CH1_2	88h
MC_SAG_CH1_3	8Ch
MC_SAG_CH1_4	90h
MC_SAG_CH1_5	94h
MC_SAG_CH1_6	98h
MC_SAG_CH1_7	9Ch
	A0h
	A4h
	A8h
	ACh
	B0h
	B4h
	B8h
	BCh
	C0h
	C4h
	C8h
	CCh
	D0h
	D4h
	D8h
	DCh
	E0h
	E4h
	E8h
	ECh
	F0h
	F4h
	F8h
	FCh

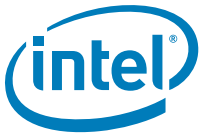


Table 2-20. Device 5, Function 2: Integrated Memory Controller Channel 1 Rank Registers

DID	VID	00h	MC_RIR_WAY_CH1_0	80h
PCISTS	PCICMD	04h	MC_RIR_WAY_CH1_1	84h
CCR	RID	08h	MC_RIR_WAY_CH1_2	88h
HDR		0Ch	MC_RIR_WAY_CH1_3	8Ch
		10h	MC_RIR_WAY_CH1_4	90h
		14h	MC_RIR_WAY_CH1_5	94h
		18h	MC_RIR_WAY_CH1_6	98h
		1Ch	MC_RIR_WAY_CH1_7	9Ch
		20h	MC_RIR_WAY_CH1_8	A0h
		24h	MC_RIR_WAY_CH1_9	A4h
		28h	MC_RIR_WAY_CH1_10	A8h
SID	SVID	2Ch	MC_RIR_WAY_CH1_11	ACh
		30h	MC_RIR_WAY_CH1_12	B0h
		34h	MC_RIR_WAY_CH1_13	B4h
		38h	MC_RIR_WAY_CH1_14	B8h
		3Ch	MC_RIR_WAY_CH1_15	BCh
MC_RIR_LIMIT_CH1_0		40h	MC_RIR_WAY_CH1_16	C0h
MC_RIR_LIMIT_CH1_1		44h	MC_RIR_WAY_CH1_17	C4h
MC_RIR_LIMIT_CH1_2		48h	MC_RIR_WAY_CH1_18	C8h
MC_RIR_LIMIT_CH1_3		4Ch	MC_RIR_WAY_CH1_19	CCh
MC_RIR_LIMIT_CH1_4		50h	MC_RIR_WAY_CH1_20	D0h
MC_RIR_LIMIT_CH1_5		54h	MC_RIR_WAY_CH1_21	D4h
MC_RIR_LIMIT_CH1_6		58h	MC_RIR_WAY_CH1_22	D8h
MC_RIR_LIMIT_CH1_7		5Ch	MC_RIR_WAY_CH1_23	DCh
		60h	MC_RIR_WAY_CH1_24	E0h
		64h	MC_RIR_WAY_CH1_25	E4h
		68h	MC_RIR_WAY_CH1_26	E8h
		6Ch	MC_RIR_WAY_CH1_27	ECh
		70h	MC_RIR_WAY_CH1_28	F0h
		74h	MC_RIR_WAY_CH1_29	F4h
		78h	MC_RIR_WAY_CH1_30	F8h
		7Ch	MC_RIR_WAY_CH1_31	FCh

Table 2-21. Device 5, Function 3: Integrated Memory Controller Channel 1 Thermal Control Registers

DID	VID	00h	MC_COOLING_COEF1	80h
PCISTS	PCICMD	04h	MC_CLOSED_LOOP1	84h
CCR	RID	08h	MC_THROTTLE_OFFSET1	88h
HDR		0Ch		8Ch
		10h		90h
		14h		94h
		18h	MC_RANK_VIRTUAL_TEMP1	98h
		1Ch	MC_DDR_THERM0_COMMAND1	9Ch
		20h	MC_DDR_THERM1_COMMAND1	A0h
		24h	MC_DDR_THERM0_STATUS1	A4h
		28h	MC_DDR_THERM1_STATUS1	A8h
SID	SVID	2Ch		ACh
		30h		B0h
		34h		B4h
		38h		B8h
		3Ch		BCh
		40h		C0h
		44h		C4h
MC_THERMAL_CONTROL1		48h		C8h
MC_THERMAL_STATUS1		4Ch		CCh
MC_THERMAL_DEFEATURE1		50h		D0h
		54h		D4h
		58h		D8h
		5Ch		DCh
MC_THERMAL_PARAMS_A1		60h		E0h
MC_THERMAL_PARAMS_B1		64h		E4h
		68h		E8h
		6Ch		ECh
		70h		F0h
		74h		F4h
		78h		F8h
		7Ch		FCh

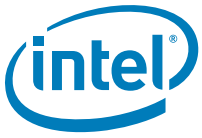


Table 2-22. Device 6, Function 0: Integrated Memory Controller Channel 2 Control Registers

DID	VID	00h	MC_CHANNEL_2_RANK_TIMING_A	80h
PCISTS	PCICMD	04h	MC_CHANNEL_2_RANK_TIMING_B	84h
CCR	RID	08h	MC_CHANNEL_2_BANK_TIMING	88h
HDR		0Ch	MC_CHANNEL_2_REFRESH_TIMING	8Ch
		10h	MC_CHANNEL_2_CKE_TIMING	90h
		14h	MC_CHANNEL_2_ZQ_TIMING	94h
		18h	MC_CHANNEL_2_RCOMP_PARAMS	98h
		1Ch	MC_CHANNEL_2_ODT_PARAMS1	9Ch
		20h	MC_CHANNEL_2_ODT_PARAMS2	A0h
		24h	MC_CHANNEL_2_ODT_MATRIX_RANK_0_3_RD	A4h
		28h	MC_CHANNEL_2_ODT_MATRIX_RANK_4_7_RD	A8h
SID	SVID	2Ch	MC_CHANNEL_2_ODT_MATRIX_RANK_0_3_WR	ACh
		30h	MC_CHANNEL_2_ODT_MATRIX_RANK_4_7_WR	B0h
		34h	MC_CHANNEL_2_WAQ_PARAMS	B4h
		38h	MC_CHANNEL_2_SCHEDULER_PARAMS	B8h
		3Ch	MC_CHANNEL_2_MAINTENANCE_OPS	BCh
		40h	MC_CHANNEL_2_TX_BG_SETTINGS	C0h
		44h		C4h
		48h	MC_CHANNEL_2_RX_BGF_SETTINGS	C8h
		4Ch	MC_CHANNEL_2_EW_BGF_SETTINGS	CCh
MC_CHANNEL_2_DIMM_RESET_CMD		50h	MC_CHANNEL_2_EW_BGF_OFFSET_SETTINGS	D0h
MC_CHANNEL_2_DIMM_INIT_CMD		54h	MC_CHANNEL_2_ROUND_TRIP_LATENCY	D4h
MC_CHANNEL_2_DIMM_INIT_PARAMS		58h	MC_CHANNEL_2_PAGETABLE_PARAMS1	D8h
MC_CHANNEL_2_DIMM_INIT_STATUS		5Ch	MC_CHANNEL_2_PAGETABLE_PARAMS2	DCh
MC_CHANNEL_2_DDR3CMD		60h	MC_TX_BG_CMD_DATA_RATIO_SETTING_CH2	E0h
		64h	MC_TX_BG_CMD_OFFSET_SETTINGS_CH2	E4h
MC_CHANNEL_2_REFRESH_THROTTLE_SUPPORT		68h	MC_TX_BG_DATA_OFFSET_SETTINGS_CH2	E8h
		6Ch		ECh
MC_CHANNEL_2_MRS_VALUE_0_1		70h	MC_CHANNEL_2_ADDR_MATCH	F0h
MC_CHANNEL_2_MRS_VALUE_2		74h		F4h
MC_CHANNEL_2_CKE_TIMING_B		78h	MC_CHANNEL_2_ECC_ERROR_MASK	F8h
MC_CHANNEL_2_RANK_PRESENT		7Ch	MC_CHANNEL_2_ECC_ERROR_INJECT	FCh

Table 2-23. Device 6, Function 1: Integrated Memory Controller Channel 2 Address Registers

DID	VID	00h	MC_SAG_CH2_0	80h
PCISTS	PCICMD	04h	MC_SAG_CH2_1	84h
CCR	RID	08h	MC_SAG_CH2_2	88h
HDR		0Ch	MC_SAG_CH2_3	8Ch
		10h	MC_SAG_CH2_4	90h
		14h	MC_SAG_CH2_5	94h
		18h	MC_SAG_CH2_6	98h
		1Ch	MC_SAG_CH2_7	9Ch
		20h		A0h
		24h		A4h
		28h		A8h
SID	SVID	2Ch		ACh
		30h		B0h
		34h		B4h
		38h		B8h
		3Ch		BCh
		40h		C0h
		44h		C4h
MC_DOD_CH2_0		48h		C8h
MC_DOD_CH2_1		4Ch		CCh
MC_DOD_CH2_2		50h		D0h
		54h		D4h
		58h		D8h
		5Ch		DCh
		60h		E0h
		64h		E4h
		68h		E8h
		6Ch		ECh
		70h		F0h
		74h		F4h
		78h		F8h
		7Ch		FCh

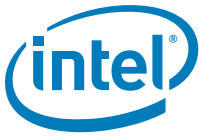


Table 2-24. Device 6, Function 2: Integrated Memory Controller Channel 2 Rank Registers

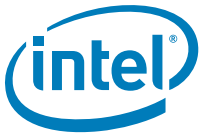
DID	VID	00h	MC_RIR_WAY_CH2_0	80h
PCISTS	PCICMD	04h	MC_RIR_WAY_CH2_1	84h
CCR	RID	08h	MC_RIR_WAY_CH2_2	88h
HDR		0Ch	MC_RIR_WAY_CH2_3	8Ch
		10h	MC_RIR_WAY_CH2_4	90h
		14h	MC_RIR_WAY_CH2_5	94h
		18h	MC_RIR_WAY_CH2_6	98h
		1Ch	MC_RIR_WAY_CH2_7	9Ch
		20h	MC_RIR_WAY_CH2_8	A0h
		24h	MC_RIR_WAY_CH2_9	A4h
		28h	MC_RIR_WAY_CH2_10	A8h
SID	SVID	2Ch	MC_RIR_WAY_CH2_11	ACh
		30h	MC_RIR_WAY_CH2_12	B0h
		34h	MC_RIR_WAY_CH2_13	B4h
		38h	MC_RIR_WAY_CH2_14	B8h
		3Ch	MC_RIR_WAY_CH2_15	BCh
MC_RIR_LIMIT_CH2_0		40h	MC_RIR_WAY_CH2_16	C0h
MC_RIR_LIMIT_CH2_1		44h	MC_RIR_WAY_CH2_17	C4h
MC_RIR_LIMIT_CH2_2		48h	MC_RIR_WAY_CH2_18	C8h
MC_RIR_LIMIT_CH2_3		4Ch	MC_RIR_WAY_CH2_19	CCh
MC_RIR_LIMIT_CH2_4		50h	MC_RIR_WAY_CH2_20	D0h
MC_RIR_LIMIT_CH2_5		54h	MC_RIR_WAY_CH2_21	D4h
MC_RIR_LIMIT_CH2_6		58h	MC_RIR_WAY_CH2_22	D8h
MC_RIR_LIMIT_CH2_7		5Ch	MC_RIR_WAY_CH2_23	DCh
		60h	MC_RIR_WAY_CH2_24	E0h
		64h	MC_RIR_WAY_CH2_25	E4h
		68h	MC_RIR_WAY_CH2_26	E8h
		6Ch	MC_RIR_WAY_CH2_27	ECh
		70h	MC_RIR_WAY_CH2_28	F0h
		74h	MC_RIR_WAY_CH2_29	F4h
		78h	MC_RIR_WAY_CH2_30	F8h
		7Ch	MC_RIR_WAY_CH2_31	FCh

Table 2-25. Device 6, Function 3: Integrated Memory Controller Channel 2 Thermal Control Registers

DID	VID	00h	MC_COOLING_COEF2	80h
PCISTS	PCICMD	04h	MC_CLOSED_LOOP2	84h
CCR	RID	08h	MC_THROTTLE_OFFSET2	88h
HDR		0Ch		8Ch
		10h		90h
		14h		94h
		18h	MC_RANK_VIRTUAL_TEMP2	98h
		1Ch	MC_DDR_THERM0_COMMAND2	9Ch
		20h	MC_DDR_THERM1_COMMAND2	A0h
		24h	MC_DDR_THERM0_STATUS2	A4h
		28h	MC_DDR_THERM1_STATUS2	A8h
SID	SVID	2Ch		ACh
		30h		B0h
		34h		B4h
		38h		B8h
		3Ch		BCh
		40h		C0h
		44h		C4h
MC_THERMAL_CONTROL2		48h		C8h
MC_THERMAL_STATUS2		4Ch		CCh
MC_THERMAL_DEFEATURE2		50h		D0h
		54h		D4h
		58h		D8h
		5Ch		DCh
MC_THERMAL_PARAMS_A2		60h		E0h
MC_THERMAL_PARAMS_B2		64h		E4h
		68h		E8h
		6Ch		ECh
		70h		F0h
		74h		F4h
		78h		F8h
		7Ch		FCh

2.5 PCI Standard Registers

These registers appear in every function for every device.



2.5.1 DID - Device Identification Register

This 16-bit register combined with the Vendor Identification register uniquely identifies the Function within the processor. Writes to this register have no effect. See Table 2-1 for the DID of each processor function.

Device: 0
Function: 0-1
Offset: 02h

Device: 2
Function: 0-5
Offset: 02h

Device: 3
Function: 0-2, 4
Offset: 02h

Device: 4-6
Function: 0-3
Offset: 02h

Bit	Type	Reset Value	Description
15:0	RO	*See Table 2-1	**Device Identification Number** Identifies each function of the processor.

2.5.2 RID - Revision Identification Register

This register contains the revision number of the processor. The Revision ID (RID) is a traditional 8-bit Read Only (RO) register located at offset 08h in the standard PCI header of every PCI/PCI Express compatible device and function.

Device: 0
Function: 0-1
Offset: 08h

Device: 2
Function: 0-5
Offset: 08h

Device: 3
Function: 0-2, 4
Offset: 08h

Device: 4-6
Function: 0-3
Offset: 08h

Bit	Type	Reset Value	Description
7:0	RO	0h	**Revision Identification Number** 0: A0 Stepping 1: B0 Stepping 2: B1 Stepping Others: RSVD

2.6 Generic Non-core Registers

2.6.1 DESIRED_CORES

Number of cores, threads BIOS wants to exist on the next reset. A processor reset must be used for this register to take affect. Note programing this register to a value higher than the product has cores, should not be done. Which cores are removed is not

defined and is implementation dependent. This does not result in all of the power savings of a reduced number of core product, but does save more power than even the deepest sleep state.

Device: 0
Function: 0
Offset: 80h
Access as a Dword

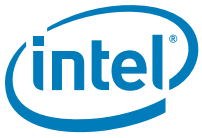
Bit	Type	Reset Value	Description
16	RW1S	0	**LOCK.** Once written to 1, changes to this register cannot be made.
8	RWL	0	**MT_DISABLE.** Disables multi-threading (2 logical threads per core) in all cores if set to 1.
2:0	RWL	0	**CORE_COUNT.** 000 - max number (default value) 001 - 1 core 010 - 2 cores 011 - 3 cores 100 - 4 cores 101 - 5 cores

2.6.2 MIRROR_PORT_CTL

Mirror Port control register.

Device: 0
Function: 0
Offset: D0h
Access as a Dword

Bit	Type	Reset Value	Description
10:7	-	-	**RESERVED**
6	RW	0	**DSBL_ENH_MPRX_SYNC.** When set, it disables the enhancing synchronization scheme for the MiP_Rx.
5	RW	0	**MIP_GO_10.** When set, the Mip_Tx and Mip_Rx go to L0 directly from Config_FlitLock.
4	RW	0	**MIP_RX_CRC_SQUASH.** When set, replaces CRC errors with CRC special packet on MiP Rx.
3	RW	0	**MIP_RX_PORT_SEL.** Port select for MiP Rx. _PORT_SEL0=QPI Port 0. _PORT_SEL1=QPI Port 1.
2	RW	0	**MIP_TX_PORT_SEL.** Port select for MiP Tx. _PORT_SEL0=QPI Port 0. _PORT_SEL1=QPI Port 1.
1	RW	1	**MIP_RX_ENABLE.** Enables the Rx portion of the mirror port.
0	RW	1	**MIP_TX_ENABLE.** Enables the Tx portion of the mirror port.



2.7 SAD - System Address Decoder Registers

2.7.1 SAD_MCSEG_BASE

Global register for MCSEG address space. These are designed to look just like the cores SMRR type registers.

Device: 0
Function: 1
Offset: 60h
Access as a Qword

Bit	Type	Reset Value	Description
63:40			**RSVD.**
39:19	RW	0	**BASE_ADDRESS.** Specifies the base address of the MCSEG. Must be aligned on 512KB or greater boundary.
18:0			**RSVD.**

2.7.2 SAD_MCSEG_MASK

Global register for MCSEG address space. These are designed to look just like the cores SMRR type registers.

Device: 0
Function: 1
Offset: 68h
Access as a Qword

Bit	Type	Reset Value	Description
63:40			**RSVD.**
39:19	RW	0	**MASK.** Specifies the mask value for the MCSEG. For initial implementations this must be a 2MB mask value = 0000_00FF_FFE0_0000 = (1FFFFCh << 19).
18:12			**RSVD.**
11	RW	0	**ENABLE.** When set to **1** all chipset accesses to this range are aborted and generate a Machine Check.
10	RW	0	**LOCK.** When set to 1 prevents modifications to the next SAD_MCSEG_BASE and SAD_MCSEG_MASK registers until the next reset.
9:0			**RSVD.**

2.7.3 SAD_MESEG_BASE

Register for ME stolen range address space. They are designed to look like the core SMRR type registers.

Device: 0 Function: 1 Offset: 70h Access as a Qword			
Bit	**Type**	**Reset Value**	**Description**
63:40			**RSVD.**
39:19	RW	0	**BASE_ADDRESS.** Specifies the base address of the MESEG. Must be aligned on 512KB or greater boundary.
18:0			**RSVD.**

2.7.4 SAD_MESEG_MASK

Register for ME stolen range address space. They are designed to look just like the core SMRR type registers.

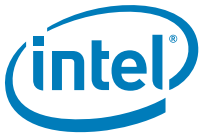
Device: 0 Function: 1 Offset: 78h Access as a Qword			
Bit	**Type**	**Reset Value**	**Description**
63:40			**RSVD.**
39:19	RW	0	**MASK.** Mask of MESEG. Space must be poewr of 2 aligned. Which bits must match the BASE in order. to be inside the ME range.
11	RW	0	**ENABLE.** Indicates if ME stolen range is enabled (when enabled all core accesses to this range are aborted).
10	RW	0	**LOCK.** Indicates if ME stolen range base/mask is locked.
11	RW	0	**ENABLE.** When set to **1** all chipset accesses to this range are aborted and generate a Machine Check.
10	RW	0	**LOCK.** When set to 1 prevents modifications to the next SAD_MCSEG_BASE and SAD_MCSEG_MASK registers until the next reset.
9:0			**RSVD.**

2.8 Intel QPI Link Registers

2.8.1 QPI_DEF_RMT_VN_CREDITS_L0
QPI_DEF_RMT_VN_CREDITS_L1

This is the control register that houses the default values of available remote credits to be transmitted to the remote agent for the remote Tx use.

Device: 2 Function: 0, 4 Offset: 58h Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
18:12	RW	100	**VNA.** VNA Credits.
11:10	RW	1	**NCS**. NCS Channel VN0 Credits.



Device: 2 Function: 0, 4 Offset: 58h Access as a Dword			
9:8	RW	1	**NCB**. NCB Channel VN0 Credits.
7:6	RW	1	**DRS**. DRS Channel VN0 Credits.
5:4	RW	1	**NDR**. NDRChannel VN0 Credits.
3:2	RW	1	**SNP**. SNP Channel VN0 Credits.
1:0	RW	1	**HOM**. HOMChannel VN0 Credits.

2.8.2 QPI_RMT_QPILP1_STAT_L0 QPI_RMT_QPILP1_STAT_L1

Remote's Intel QPI Parameter 1 Value register.

Device: 2 Function: 0, 4 Offset: C4h Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
11		-	**BP_Request.** Indicates whether the remote agent is requesting backpressure during L1 state.
10		-	**BP_Support.** Indicates the remote agent's ability to support backpressure during L1 state.
9	RO	-	**L1_SUPPORT**. Indicates the remote agent's ability to support L1 state.
8	RO	-	**L0P_SUPPORT**. Indicates the remote agent's ability to support L0P state.
7	RO	-	**L0S_SUPPORT**. Indicates the remote agent's ability to support L0S state.
6	RO	-	**RX_CII_SUPPORT**. Indicates the remote agent's ability to receive CII data.
5	RO	-	**PREFERRED_TX_SDI_MODE**. Indicates the ability of the remote agent transmitter to send scheduled data interleave data.
4	RO	-	**RCV_SDI_SUPPORT**. Indicates remote agent can receive scheduled data interleave data.
3:2	RO	-	**PREFERRED_TX_CRC_MODE**. Preferred send mode for the remote transmitter. 00: No CRC 01: 8b CRC 10: 16b rolling CRC 11: RSVD
1:0	RO	-	**RCV_CRC_MODE_SUPPORTED**. CRC modes that the remote agent supports. 00: RSVD 01: 8b CRC 10: 16b and 8b CRC 11: RSVD

2.8.3 MIP_PH_CTR_L0 MIP_PH_CTR_L1

Mirror Port Physical Layer Control Register.

Device: 2 Function: 2,3 Offset: 6Ch Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
31	RW	0	**RETRAIN_NOW.** This bit generates a retraining event with the provided retraining parameters when enabled only during at-speed operation**.**
27	RW	0	**LA_LOAD_DISABLE.** Disables the loading of the effective values of the Intel® QuickPath CSRs when set.
23	RW	0	**ENABLE_PRBS.** Enables LFSR pattern during bitlock/training.
22	RW	0	**ENABLE_SCRAMBLE.** Enables data scrambling through LFSR.
14	RW	1	**DETERMINISM_MODE.** Sets determinism mode of operation.
13	RW	1	**DISABLE_AUTO_COMP.** Disables automatic entry into compliance.
12	RW	0	**INIT_FREEZE.** When set, freezes the FSM when initialization aborts.
10:8	RW	0	**INIT_MODE.** Initialization mode that determines altered initialization modes.
7	RW	0	**LINK_SPEED.** Identifies slow speed or at-speed operation for the Intel QPI port.
5	RW	1	**PHYINITBEGIN.** Instructs the port to start initialization.
4	RW	0	**SINGLE_STEP.** Enables single step mode.
3	RW	0	**LAT_FIX_CTL.** If set, instructs the remote agent to fix the latency.
2	RW	0	**BYPASS_CALIBRATION.** Indicates the physical layer to bypass calibration.
1	RW	0	**RESET_MODIFIER.** Modifies soft reset to default reset when set.
0	RW1S	0	**PHY_RESET. Physical Layer Reset.** Note while this register is locked after going to FAST speed L0, this bit is not locked.

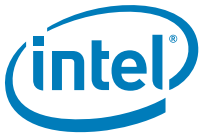
2.8.4 MIP_PH_PRT_L0
MIP_PH_PRT_L1

Mirror Port periodic retraining timing register.

Device: 2 Function: 2,3 Offset: A4h Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
21:16	RW	29	**RETRAIN_PKT_CNT.** Retraining packet count.
13:10	RW	11	**EXP_RETRAIN_INTERVAL.** Exponential count for retraining interval.
7:0	RW	3	**RETRAIN_INTERVAL.** Periodic retraining interval. A value of 0 indicates retraining is disabled.

2.9 Integrated Memory Controller Control Registers

The registers in this section apply only to processors supporting registered DIMMs



2.9.1 MC_SMI_DIMM_ERROR_STATUS

SMI DIMM error threshold overflow status register. This bit is set when the per-DIMM error counter exceeds the specified threshold. The bit is reset by BIOS.

Device: 3
Function: 0
Offset: 50h
Access as a Dword

Bit	Type	Reset Value	Description
13:12	RW0C	0	**REDUNDANCY_LOSS_FAILING_DIMM**. The ID for the failing DIMM when redundancy is lost.
11:0	RW0C	0	**DIMM_ERROR_OVERFLOW_STATUS.** This 12-bit field is the per dimm error overflow status bits. The organization is as follows: If there are three or more DIMMS on the channel: Bit 0 : Dimm 0 Channel 0 Bit 1 : Dimm 1 Channel 0 Bit 2 : Dimm 2 Channel 0 Bit 3 : Dimm 3 Channel 0 Bit 4 : Dimm 0 Channel 1 Bit 5 : Dimm 1 Channel 1 Bit 6 : Dimm 2 Channel 1 Bit 7 : Dimm 3 Channel 1 Bit 8 : Dimm 0 Channel 2 Bit 9 : Dimm 1 Channel 2 Bit 10 : Dimm 2 Channel 2 Bit 11 : Dimm 3 Channel 2 If there are one or two DIMMS on the channel: Bit 0 : Dimm 0, Ranks 0 and 1, Channel 0 Bit 1 : Dimm 0, Ranks 2 and 3, Channel 0 Bit 2 : Dimm 1, Ranks 0 and 1, Channel 0 Bit 3 : Dimm 1, Ranks 2 and 3, Channel 0 Bit 4 : Dimm 0, Ranks 0 and 1, Channel 1 Bit 5 : Dimm 0, Ranks 2 and 3, Channel 1 Bit 6 : Dimm 1, Ranks 0 and 1, Channel 1 Bit 7 : Dimm 1, Ranks 2 and 3, Channel 1 Bit 8 : Dimm 0, Ranks 0 and 1, Channel 2 Bit 9 : Dimm 0, Ranks 2 and 3, Channel 2 Bit 10 : Dimm 1, Ranks 0 and 1, Channel 2 Bit 11 : Dimm 1, Ranks 2 and 3, Channel 2

2.9.2 MC_SMI__CNTRL

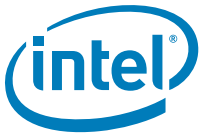
System Management Interrupt control register.

Device: 3 Function: 0 Offset: 54h Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
16	RW	0	**INTERRUPT_SELECT_NMI.** NMI enable. Set to enable NMI signaling. Clear to disable NMI signaling. If both NMI and SMI enable bits are set, then only SMI is sent.
15	RW	0	**INTERRUPT_SELECT_SMI.** SMI enable. Set to enable SMI signaling. Clear to disable SMI signaling. If both NMI and SMI enable bits are set, then only SMI is sent. This bit functions the same way in Mirror and Independent Modes. The possible SMI events enabled by this bit are: Any one of the error counters MC_COR_ECC_CNT_X meets the value of SMI_ERROR_THRESHOLD field of this register. MC_RAS_STATUS.REDUNDANCY_LOSS bit is set to 1.
14:0	RW	0	**SMI_ERROR_THRESHOLD.** Defines the error threshold to compare against the per-DIMM error counters MC_COR_ECC_CNT_X, which are also 15 bits.

2.9.3 MC_MAX_DOD

Defines the MAX number of DIMMS, RANKS, BANKS, ROWS, COLS among all DIMMS populating the three channels. The Memory Init logic uses this register to cycle through all the memory addresses writing all 0's to initialize all locations. This register is also used for scrubbing and must always be programmed if any DODs are programmed.

Device: 3 Function: 0 Offset: 64h Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
10:9	RW	0	**MAXNUMCOL.** Maximum Number of Columns. 00: 2^10 columns 01: 2^11 columns 10: 2^12 columns 11: RSVD.
8:6	RW	0	**MAXNUMROW.** Maximum Number of Rows. 000: 2^12 Rows 001: 2^13 Rows 010: 2^14 Rows 011: 2^15 Rows 100: 2^16 Rows Others: RSVD.
5:4	RW	0	**MAXNUMBANK.** Max Number of Banks. 00: Four-banked 01: Eight-banked 10: Sixteen-banked.
3:2	RW	0	**MAXNUMRANK.** Maximum Number of Ranks. 00: Single Ranked 01: Double Ranked 10: Quad Ranked.



Device: 3 Function: 0 Offset: 64h Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
1:0	RW	0	**MAXNUMDIMMS.** Maximum Number of Dimms. 00: 1 Dimm 01: 2 Dimms 10: 3 Dimms 11: RSVD.

2.9.4 MC_RD_CRDT_INIT

These registers contain the initial read credits available for issuing memory reads. TAD read credit counters are loaded with the corresponding values at reset and anytime this register is written. BIOS must initialize this register with appropriate values depending on the level of Isoch support in the platform. It is illegal to write this register while TAD is active (has memory requests outstanding), as the write will break TAD's outstanding credit count values.

Register programming rules:

- Total read credits (CRDT_RD + CRDT_RD_HIGH + CRDT_RD_CRIT) must not exceed 31.
- CRDT_RD_HIGH value must correspond to the number of high RTIDs reserved at the IOH.
- CRDT_RD_CRIT value must correspond to the number of critical RTIDs reserved at the IOH.
- CRDT_RD_HIGH + CRDT_RD must be less than or equal to 13 if High or Critical credits are nonzero.
- CRDT_RD_HIGH + CRDT_RD_CRIT must be less than or equal to 8.
- CRDT_RD_CRIT must be less than or equal to 6. Set CRDT_RD to (16 - CRDT_RD_CRIT - CRDT_RD_HIGH).
- If (Mirroring enabled) then Max for CRDT_RD is 14, otherwise it is 15.
- If (Isoch not enabled) then CRDT_RD_HIGH and CRDT_RD_CRIT are set to 0.

Device: 3 Function: 0 Offset: 70h Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
20:16	RW	3	**CRDT_RD_CRIT.** Critical Read Credits.
12:8	RW	1	**CRDT_RD_HIGH.** High Read Credits.
4:0	RW	13	**CRDT_RD.** Normal Read Credits.

2.9.5 MC_SCRUBADDR_HI

This register pair contains part of the address of the last patrol scrub request issued. When running memtest, the failing address is logged in this register on memtest errors. Software can write the next address into this register. Scrubbing must be disabled to reliably read and write this register.

Device: 3
Function: 0
Offset: 7Ch
Access as a Dword

Bit	Type	Reset Value	Description
12	RO	0	**MEMBIST_INPROGRESS**. When this bit is asserted by hardware MemTest/MemInit is in progress.
11	RO	0	**MEMBIST_CMPLT.** When this bit is asserted by hardware MemTest/MemInit is complete.
10	WO	0	**RESET_MEMBIST_STATUS**. When this bit is written to a 1, the status field MEMBIST_CMPLT is cleared.
9:8	RW	0	**CHNL.** Can be written to specify the next scrub address with STARTSCRUB in the MC_SCRUB_CONTROL register. Contains the channel address of the last patrol scrub issued.
7:6	RW	0	**DIMM.** Contains the dimm of the last scrub issued. Can be written to specify the next scrub address with STARTSCRUB in the MC_SCRUB_CONTROL register.
5:4	RW	0	**RANK.** Contains the rank of the last scrub issued. Can be written to specify the next scrub address with STARTSCRUB in the MC_SCRUB_CONTROL register.
3:0	RW	0	**BANK**. Contains the bank of the last scrub issued. Can be written to specify the next scrub address with STARTSCRUB in the MC_SCRUB_CONTROL register.

2.10 Integrated Memory Controller RAS Registers

2.10.1 MC_SSRCONTROL

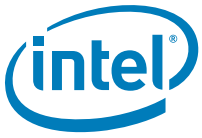
scrubbing control. This register allows the enabling of sparing, patrol scrubbing and demand scrubbing.

Device: 3
Function: 2
Offset: 48h
Access as a Dword

Bit	Type	Reset Value	Description
14:7	RW	0	**SCRATCHPAD.** This field is available as a scratchpad for Scrubbing operations.
6	RW	0	**DEMAND_SCRUB_EN.** Enable Demand Scrubs.
1:0	RW	0	**SSR_MODE.** Spare control enable. 00: Idle 01: Scrub 10: Spare

2.10.2 MC_SCRUB_CONTROL

Contains the Scrub control parameters and status.



Device: 3 Function: 2 Offset: 4Ch Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
29:27	RW	0	**SKIP_SCRUB.** This bit disables patrol scrubs to the channel corresponding to the bit that is set. Bit 27 disables patrol scrubs to channel 0, bit 28 disables patrol scrubs to channel 1 and bit 29 disables patrol scrubs to channel 2. This bit can only be set or reset on a system with patrol scrub enabled, and only after transitioning the SSR_CONTROL.SSR_MODE to idle and polling until SSRSTATUS.CMPLT is 1. When mirroring is enabled this field must not be set.
26	RW	0	**SCRUBISSUED.** When Set, the scrub address registers contain the last scrub address issued.
25	-	-	**RSVD**.
24	RW	0	**STARTSCRUB.** When Set, the Patrol scrub engine will start from the address in the scrub address registers. Once the scrub is issued this bit is reset.
23:0	RW	0	**SCRUBINTERVAL.** Defines the interval in DCLKS between patrol scrub requests. The calculation for this register to get a scrub to every line in 24 hours is: ((36400)/(memory capacity/64))/cycle time of DCLK For 512MB at DDR3-800: (36400/((2^29)/64))/1.25 x 10^-9 = 3471374 = 0x34F80E

2.10.3 MC_SSRSTATUS

Provides the status of the operation specified in MC_SSRCONTROL.SSR_Mode.

Device: 3 Function: 2 Offset: 60h Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
1	RO	0	**INPROGRESS.** Patrol Scrub operation in progress. This bit is set by hardware once scrubbing operation has started. It is cleared once operation is complete or fails.
0	RO	0	**CMPLT.** Patrol Scrub operation complete. Set by hardware once operation is complete. Bit is cleared by hardware when a new operation is enabled.

2.11 Integrated Memory Controller Channel Control Registers

2.11.1 MC_CHANNEL_0_REFRESH_THROTTLE_SUPPORT
MC_CHANNEL_1_REFRESH_THROTTLE_SUPPORT
MC_CHANNEL_2_REFRESH_THROTTLE_SUPPORT

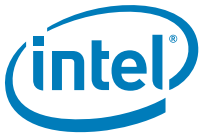
This register supports Self Refresh and Thermal Throttle functions.

Device: 4, 5, 6 Function: 0 Offset: 68h Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
5	RW	0	**RSVD.**
4	RW	0	**RSVD.**
3:2	RW	0	**INC_ENTERPWRDWN_RATE.** Powerdown rate will be increased during thermal throttling based on the following configurations. 00: tRANKIDLE (Default) 01: 16 10: 24 11: 32
1	RW	0	**DIS_OP_REFRESH**. When set, the refresh engine will not issue opportunistic refresh.
0	RW	0	**ASR_PRESENT.** When set, indicates DRAMs on this channel can support Automatic Self Refresh. If the DRAM is not supporting ASR (Auto Self Refresh), then Self Refresh entry will be delayed until the temperature is below the 2x refresh temperature.

2.11.2 MC_CHANNEL_0_RANK_TIMING_A
MC_CHANNEL_1_RANK_TIMING_A
MC_CHANNEL_2_RANK_TIMING_A

This register contains parameters that specify the rank timing used. All parameters are in DCLK.

Device: 4, 5, 6 Function: 0 Offset: 80h Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
28:26	RW	0	**tddWrTRd.** Minimum delay between a write followed by a read to different DIMMs. 000: 1 001: 2 010: 3 011: 4 100: 5 101: 6 110: 7 111: 8
25:23	RW	0	**tdrWrTRd.** Minimum delay between a write followed by a read to different ranks on the same DIMM. 000: 1 001: 2 010: 3 011: 4 100: 5 101: 6 110: 7 111: 8

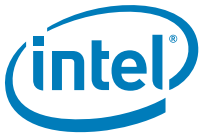


Device: 4, 5, 6 Function: 0 Offset: 80h Access as a Dword			
22:19	RW	0	**tsrWrTRd.** Minimum delay between a write followed by a read to the same rank. 0000: 10 0001: 11 0010: 12 0011: 13 0100: 14 0101: 15 0110: 16 0111: 17 1000: 18 1001: 19 1010: 20 1011: 21 1100: 22 1101: 23 1110: 24 1111: 25
18:15	RW	0	**tddRdTWr.** Minimum delay between Read followed by a Write to different DIMMs. 0000: 2 0001: 3 0010: 4 0011: 5 0100: 6 0101: 7 0110: 8 0111: 9 1000: 10 1001: 11 1010: 12 1011: 13 1100: 14 1101: RSVD 1110: RSVD 1111: RSVD
14:11	RW	0	**tdrRdTWr.** Minimum delay between Read followed by a write to different ranks on the same DIMM. 0000: 2 0001: 3 0010: 4 0011: 5 0100: 6 0101: 7 0110: 8 0111: 9 1000: 10 1001: 11 1010: 12 1011: 13 1100: 14 1101: RSVD 1110: RSVD 1111: RSVD

Device: 4, 5, 6 Function: 0 Offset: 80h Access as a Dword			
10:7	RW	0	**tsrRdTWr.** Minimum delay between Read followed by a write to the same rank. 0000: RSVD 0001: RSVD 0010: RSVD 0011: 5 0100: 6 0101: 7 0110: 8 0111: 9 1000: 10 1001: 11 1010: 12 1011: 13 1100: 14 1101: RSVD 1110: RSVD 1111: RSVD
6:4	RW	0	**tddRdTRd.** Minimum delay between reads to different DIMMs. 000: 2 001: 3 010: 4 011: 5 100: 6 101: 7 110: 8 111: 9
3:1	RW	0	**tdrRdTRd.** Minimum delay between reads to different ranks on the same DIMM. 000: 2 001: 3 010: 4 011: 5 100: 6 101: 7 110: 8 111: 9
0	RW	0	**tsrRdTRd.** Minimum delay between reads to the same rank. 0: 4 1: 6

2.11.3 MC_CHANNEL_0_REFRESH_TIMING
MC_CHANNEL_1_REFRESH_TIMING
MC_CHANNEL_2_REFRESH_TIMING

This register contains parameters that specify the refresh timings. Units are in DCLK.



Device: 4, 5, 6 Function: 0 Offset: 8Ch Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
29:19	RW	0	**tTHROT_OPPREF.** The minimum time between two opportunistic refreshes. Should be set to tRFC in DCLKs. Zero is an invalid encoding. A value of 1 should be programmed to disable the throttling of opportunistic refreshes. By setting this field to tRFC, current to a single DIMM can be limited to that required to support this scenario without significant performance impact: - 8 panic refreshes in tREFI to one rank - 1 opportunistic refresh every tRFC to another rank - full bandwidth delivered by the third and fourth ranks Platforms that can supply peak currents to the DIMMs should disable opportunistic refresh throttling for maximum performance.
18:9	RW	0	**tREFI_8.** Average periodic refresh interval divided by 8.
8:0	RW	0	**tRFC.** Delay between the refresh command and an activate or refresh command.

2.11.4 MC_CHANNEL_0_CKE_TIMING
MC_CHANNEL_1_CKE_TIMING
MC_CHANNEL_2_CKE_TIMING

This register contains parameters that specify the CKE timings. All units are in DCLK.

Device: 4, 5, 6 Function: 0 Offset: 90h Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
21	RW	1	**CsForCkeTransition.** Specifies if CS is to be asserted when CKE transition with PowerDown entry/exit and SelfRefresh exit.
20:11	RW	0	**tXSDLL.** Minimum delay between the exit of self refresh and commands that require a locked DLL.
10:3	RW	0	**tXS.** Minimum delay between the exit of self refresh and commands not requiring a DLL.
2:0	RW	0	**tCKE.** CKE minimum pulse width.

2.11.5 MC_CHANNEL_0_CKE_TIMING_B
MC_CHANNEL_1_CKE_TIMING_B
MC_CHANNEL_2_CKE_TIMING_B

This register contains parameters that specify CKE timings.

Device: 4, 5, 6 Function: 0 Offset: 78h Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
14:5	RW	0	**tRANKIDLE:** Rank will go into powerdown after it has been idle for the specified number of DCLKs. tRANKIDLE covers max(txxxPDEN). Minimum value is tWRAPDEN. If CKE is being shared between ranks then both ranks must be idle for this amount of time. A Power Down Entry command will be requested for a rank after this number of DCLKs if no request to the rank is in the MC.
4:0	RW	0	**tXP.** Minimum delay from exit power down with DLL and any valid command. Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL.

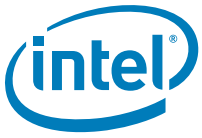
2.11.6 MC_CHANNEL_0_SCHEDULER_PARAMS MC_CHANNEL_1_SCHEDULER_PARAMS MC_CHANNEL_2_SCHEDULER_PARAMS

These are the parameters used to control parameters within the scheduler.

Device: 4, 5, 6 Function: 0 Offset: B8h Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
14	RW	0	**DISABLE_8B_CRITICAL_WORD.** Disable critical word first optimization
13	RW	0	**DDR_CLK_TRISTATE_DISABLE.** When 0, DDR clock drivers will always be enabled.
12	RW	0	**CS_ODT_TRISTATE_DISABLE**. When set low(0) CS and ODT drivers will always be enabled.
11	RW	0	**FLOAT_EN**. When set, the address and command lines will float to save power when commands are not being sent out.
10:6	RW	7	**PRECASRDTHRESHOLD.** Threshold above which Medium-Low Priority reads can PRE-CAS write requests.
5	RW	0	**DISABLE_ISOC_RBC_RESERVE.** When set this bit will prevent any RBC's from being reserved for ISOC.
3	RW	0	**ENABLE2N.** Enable 2n Timing.
2:0	RW	0	**PRIORITYCOUNTER.** Upper 3 MSB of 8 bit priority time out counter.

2.11.7 MC_CHANNEL_0_PAGETABLE_PARAMS2 MC_CHANNEL_1_PAGETABLE_PARAMS2 MC_CHANNEL_2_PAGETABLE_PARAMS2

These are the parameters used to control parameters for page closing policies.



Device: 4, 5, 6 Function: 0 Offset: DCh Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
27	RW	0	**ENABLEADAPTIVEPAGECLOSE**. When set, enables Adaptive Page Closing.
26:18	RW	0	**MINPAGECLOSELIMIT**. Upper 9 MSBs of a 13-bit threshold limit. When the mistake counter falls below this threshold, a less aggressive page close interval (larger) is selected.
17:9	RW	0	**MAXPAGECLOSELIMIT**. Upper 9 bits of a 13-bit threshold limit. When the mistake counter exceeds this threshold, a more aggressive page close interval (smaller) is selected.
8:0	RW	0	**MISTAKECOUNTER.** Upper 8 MSBs of a 12-bit counter. This counter adapts the interval between assertions of the page close flag. For a less aggressive page close, the length of the count interval is increased and vice versa for a more aggressive page close policy.

2.12 Memory Thermal Control

2.12.1 MC_THERMAL_STATUS0 MC_THERMAL_STATUS1 MC_THERMAL_STATUS2

Status registers for the thermal throttling logic for each channel.

Device: 4, 5, 6 Function: 3 Offset: 4Ch Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
29:4	RO	0	**CYCLES_THROTTLED.** The number of throttle cycles, in increments of 256 Dclks, triggered in any rank in the last SAFE_INTERVAL number of ZQs.
3:0	RO	0	**RANK_TEMP.** The bit[3:0] specifies whether the throttler[3:0] is above throttling threshold**.**

2.12.2 MC_DDR_THERM0_COMMAND0 MC_DDR_THERM0_COMMAND1 MC_DDR_THERM0_COMMAND2

This register contains the command portion of the DDR_THERM# pin functionality (i.e. what an assertion of the pin does).

Device: 4, 5, 6 Function: 3 Offset: 9Ch Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
3	RW	0	**THROTTLE.** Force throttling when DDR_THERM# pin is asserted.

Device: 4, 5, 6 Function: 3 Offset: 9Ch Access as a Dword			
2	RW	0	**REF_2X.** Force 2x refresh as long as DDR_THERM# is asserted (low).
1	RW	0	**DISABLE_EXTTS.** Response to DDR_THERM# pin is disabled. ASSERTION and DEASSERTION fields in the register MC_DDR_THERM0_STATUS are frozen.
0	RW1S	0	**LOCK.** When set, all bits in this register are RO and cannot be written. Reset will clear the lock.

2.12.3 MC_DDR_THERM1_COMMAND0 MC_DDR_THERM1_COMMAND1 MC_DDR_THERM1_COMMAND2

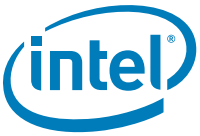
This register contains the command portion of the DDR_THERM2# pin functionality (i.e. what an assertion of the pin does).

Device: 4, 5, 6 Function: 3 Offset: A0h Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
3	RW	0	**THROTTLE.** Force throttling when DDR_THERM# pin is asserted.
2	RW	0	**REF_2X.** Force 2x refresh as long as DDR_THERM# is asserted (low).
1	RW	0	**DISABLE_EXTTS.** Response to DDR_THERM# pin is disabled. ASSERTION and DEASSERTION fields in the register MC_DDR_THERM_STATUS are frozen.
0	RW1S	0	**LOCK.** When set, all bits in this register are RO and cannot be written. Reset will clear the lock.

2.12.4 MC_DDR_THERM0_STATUS0 MC_DDR_THERM0_STATUS1 MC_DDR_THERM0_STATUS2

This register contains the status portion of the DDR_THERM# pin functionality (that is, what is happening or has happened with respect to the pin).

Device: 4, 5, 6 Function: 3 Offset: A4h Access as a Dword			
Bit	**Type**	**Reset Value**	**Description**
2	RO	0	**ASSERTION.** An assertion edge was seen on DDR_THERM#. Write-1-to-clear.
1	RO	0	**DEASSERTION.** A de-assertion edge was seen on DDR_THERM#. Write-1-to-clear.
0	RO	0	**STATE.** Present logical state of DDR_THERM# bit. This is a static indication of the pin, and may be several clocks out of date due to the delay between the pin and the signal. STATE = 0 means DDR_THERM# is deasserted STATE = 1 means DDR_THERM# is asserted



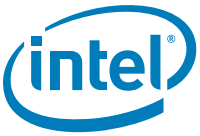
2.12.5 MC_DDR_THERM1_STATUS0 MC_DDR_THERM1_STATUS1 MC_DDR_THERM1_STATUS2

This register contains the status portion of the DDR_THERM2# pin functionality (that is, what is happening or has happened with respect to the pin).

Device: 4, 5, 6
Function: 3
Offset: A8h
Access as a Dword

Bit	Type	Reset Value	Description
2	RO	0	**ASSERTION.** An assertion edge was seen on DDR_THERM#. Write-1-to-clear.
1	RO	0	**DEASSERTION.** A de-assertion edge was seen on DDR_THERM#. Write-1-to-clear.
0	RO	0	**STATE.** Present logical state of DDR_THERM# bit. This is a static indication of the pin, and may be several clocks out of date due to the delay between the pin and the signal. STATE = 0 means DDR_THERM# is deasserted STATE = 1 means DDR_THERM# is asserted

§



3 Functional Description

This chapter describes the functional differences between the Intel Xeon processor 5500 series and Intel Xeon processor 5600 series. For more information on the Intel Xeon processor 5500 series features and functionality, refer to the *Intel® Xeon® Processor 5500 Series Datasheet, Volume 2*.

3.1 Integrated Memory Controller

The Intel Xeon processor 5600 series integrated memory controller supports DDR3 800, DDR3 1066 and DDR3 1333 memory technologies. Below is a comparison of Intel Xeon processor 5500 series and Intel Xeon processor 5600 series memory controller features.

Table 3-1. Integrated Memory Controller Feature Comparison (Sheet 1 of 2)

Feature	Intel® Xeon® Processor 5500 Series	Intel® Xeon® Processor 5600 Series
DRAM Technology	DDR3	
DIMM Technology	RDIMM, UDIMM (1.5 V)	RDIMM, UDIMM (1.5 V and 1.35 V)
DIMM Raw Cards	RDIMM Raw Cards as defined by JEDEC: A(1Rx8), B(2Rx8), C(1Rx4), D(2Rx4), E/J(2Rx4), F/AB(4Rx4), H(4Rx8) UDIMM Raw Cards as defined by JEDEC: A(1Rx8), B(2Rx8), C(1Rx16), D(1Rx8 w/ ECC), E(2Rx8 w/ ECC)	RDIMM Raw Cards as defined by JEDEC: A(1Rx8), B(2Rx8), C(1Rx4), D(2Rx4), E/J(2Rx4), F/AB(4Rx4), H(4Rx8), D(2Rx4) UDIMM Raw Cards as defined by JEDEC: A(1Rx8), B(2Rx8), C(1Rx16), D(1Rx8 w/ ECC), E(2Rx8 w/ ECC)
Max Physical Channels per Socket	3	
Max DIMMs per channel	2-3 RDIMMs, 2 UDIMMs	
Max Speed	800, 1066, or 1333 MT/s	
Max #of Ranks per Channel	8	
Banks per Rank	8	
DRAM Sizes	1 Gb, 2 Gb	1 Gb, 2 Gb, 4 Gb[5]
Ranks per DIMM	1,2,4	
Data lines per DRAM	RDIMM: x4,x8; UDIMM: x8 and x16[1]	
Max Memory Supported per Platform	**RDIMM:** 72 GB (1Rank, 18x4 GB, @800 MT/s); 144 GB (2Rank, 18x8 GB, @800 MT/s); 192 GB (4Rank, 12x16 GB, @800 MT/s) **UDIMM:** 24 GB (1Rank, 12x2 GB, @1066 MT/s); 48 GB (2Rank, 12x4 GB @1066 MT/s)	**RDIMM:** 72 GB (1Rank, 18x4 GB, @800 MT/s); 288 GB (2Rank, 18x 16 GB, @800 MT/s); 192 GB (4Rank, 12x16 GB, @800 MT/s) **UDIMM:** 24 GB (1Rank, 12x2 GB, @1066 MT/s); 48 GB (2Rank, 12x4 GB @1066 MT/s)
Address Fault Detection	Address Parity	
Page Policy	Open and Closed Page	
Intel® TXT (Trusted Execution)	No	Yes
ECC Support	Yes	
Independent Channel Support	Yes	
RAS - Lockstep Channel Support	Only Channel 0 and 1 can be populated. Not supported with Mirroring	Only Channel 0 and 1 can be populated. Not supported with Mirroring

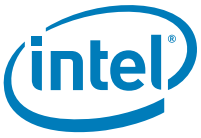


Table 3-1. Integrated Memory Controller Feature Comparison (Sheet 2 of 2)

Feature	Intel® Xeon® Processor 5500 Series	Intel® Xeon® Processor 5600 Series
RAS - Sparing Channel Support	No	Yes. Channel 2 can be used as a spare for channels on the same socket. All channels must be identically populated. Not supported when in Lockstep Mode
RAS - Mirroring Channel Support	Yes. Between Ch 0 and Ch 1 of the same socket. Ch2 may not be populated. Not with lockstep.	Yes. Between Ch 0 and Ch 1 of the same socket. Ch2 may not be populated. Not with lockstep.
RAS - Demand and Patrol Scrubbing	Yes	
RAS - SDDC (Single Device Data Correction) Support	**RDIMMs:** x4 SDDC in Independent Channel Mode; x8 SDDC in Lockstep Mode. **UDIMM w/ECC:** x8 SDDC in Lockstep Mode with x8 UDIMMs only	
Active Powerdown	Per rank for up to 4 ranks. Ranks share CKE for >4 ranks	
Precharge Power Down	Per rank. No support for turning off DRAM DLLs	
Self Refresh	In Package C3, C6 states and during S3	
Clocks off in Package Cstates	Yes - C3, C6	
Memory Init	RDIMMs: Yes UDIMMs: When ECC DIMMs are present	
Memory Test	Yes when ECC DIMMs are present.	
Poisoning	Yes	

Notes:

1. x16 DRAM is not supported on RDIMM/UDIMM combo design.

3.2 Supported RDIMM Memory Configurations

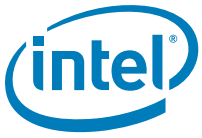
3.2.1 RDIMM 1.5 V Configurations

Table 3-2. RDIMM (1.5 V) Support

DIMM Slots per Channel	DIMMS Populated per Channel	DIMM Type	POR Speeds	Ranks per DIMM (any combination)
2	1	Reg. DDR3 ECC	800, 1066, 1333	SR or DR
2	1	Reg. DDR3 ECC	800, 1066	QR only
2	2	Reg. DDR3 ECC	800, 1066, 1333	Mixing SR, DR
2	2	Reg. DDR3 ECC	800	Mixing SR, DR, QR
3	1	Reg. DDR3 ECC	800, 1066, 1333	SR or DR
3	1	Reg. DDR3 ECC	800, 1066	QR only
3	2	Reg. DDR3 ECC	800, 1066, 1333	Mixing SR, DR
3	2	Reg. DDR3 ECC	800	Mixing SR, DR, QR
3	3	Reg. DDR3 ECC	800	Mixing SR, DR

Notes:

1. The Intel Xeon processor 5600 series supports all Intel Xeon processor 5500 series memory configurations.
2. Any combination of x4 and x8 RDIMMs, with 1Gb, 2Gb, or 4Gb DRAM density, is supported.
3. Populate DIMMs starting with slot 0, furthest from the CPU.



3.2.2 RDIMM 1.35 V Configurations

Table 3-3. RDIMM (1.35 V) Support

DIMM Slots per Channel	DIMMS Populated per Channel	DIMM Type	POR Speeds	Ranks per DIMM (any combination)
2	1	Reg. DDR3L 1.35 V ECC	800, 1066, 1333	SR or DR
2	1	Reg. DDR3L 1.35 V ECC	800	QR only
2	2	Reg. DDR3L 1.35 V ECC	800, 1066	Mixing SR, DR
2	2	Reg. DDR3L 1.35 V ECC	800	Mixing SR, DR, QR
3	1	Reg. DDR3L 1.35 V ECC	800, 1066, 1333	SR or DR
3	1	Reg. DDR3L 1.35 V ECC	800	QR only
3	2	Reg. DDR3L 1.35 V ECC	800, 1066	Mixing SR, DR
3	2	Reg. DDR3L 1.35 V ECC	800	Mixing SR, DR, QR

Notes:
1. The Intel Xeon processor 5600 series supports all timings defined by the JEDEC standard.
2. All channels in a system will run at the fastest common frequency.
3. Mixing of registered and unbuffered DIMMs is not supported.
4. If 1.35V and 1.5V DIMMs are mixed, the DIMMs will run at 1.5V.

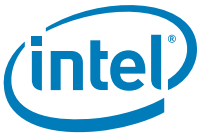
3.3 Supported UDIMM Memory Configurations

3.3.1 UDIMM 1.5V Configurations

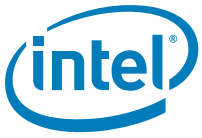
Table 3-4. UDIMM (1.5V) Support

Platforms with UDIMM Only Routing					
DIMM Slots per Channel	**DIMMs Populated per Channel**	**DIMM Type**	**POR Speeds**	**Ranks per DIMM (any combination)**	**Notes**
2	1	Unbuffered DDR3 (w/ or w/o ECC)	800, 1066, 1333	SR or DR	1,2,3,5
2	2	Unbuffered DDR3 (w/ or w/o ECC)	800, 1066, 1333	Mixing SR, DR	
Platforms with Combo UDIMM/RDIMM 3 DIMMs per Channel Routing					
DIMM Slots per Channel	**DIMMs Populated per Channel**	**DIMM Type**	**POR Speeds**	**Ranks per DIMM (any combination)**	**Notes**
3	1	Unbuffered DDR3 (w/ or w/o ECC)	800, 1066, 1333	SR or DR	1,3,4,5
3	2	Unbuffered DDR3 (w/ or w/o ECC)	800, 1066, 1333	Mixing SR, DR	

Notes:



1. The Intel Xeon processor 5600 series supports all Intel Xeon processor 5500 series POR memory configurations.
2. Any combination of x8 and x16 UDIMMs, with 1Gb or 2Gb DRAM density, is supported.
3. Populate DIMMs starting with slot 0, furthest from the CPU.
4. Any combination of x8 UDIMMs, with 1Gb or 2Gb DRAM density, is supported.
5. 2 DIMMs Populated per Channel at 1333 MT/s is only supported on UDIMMs with ECC support.



3.3.2 UDIMM 1.35V Configurations

Table 3-5. UDIMM (1.35V) Support

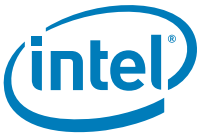
Platforms with UDIMM Only Routing					
DIMM Slots per Channel	**DIMMs Populated per Channel**	**DIMM Type**	**POR Speeds**	**Ranks per DIMM (any combination)**	**Notes**
2	1	Unbuffered DDR3L 1.35V (w/ ECC)	800, 1066, 1333	SR or DR	1-7
2	2	Unbuffered DDR3L 1.35V (w/ ECC)	800, 1066	Mixing SR, DR	
Platforms with Combo UDIMM/RDIMM 3 DIMMs per Channel Routing					
DIMM Slots per Channel	**DIMMs Populated per Channel**	**DIMM Type**	**POR Speeds**	**Ranks per DIMM (any combination)**	**Notes**
3	1	Unbuffered DDR3L 1.35V (w/ ECC)	800, 1066, 1333	SR or DR	1-5, 7,8
3	2	Unbuffered DDR3L 1.35V (w/ ECC)	800, 1066	Mixing SR, DR	

Notes:
1. The Intel Xeon processor 5600 series supports all timings defined by the JEDEC standard.
2. All channels in a system will run at the fastest common frequency.
3. Mixing of registered and unbuffered DIMMs is not supported.
4. The Intel Xeon processor 5600 series and DDR3L UDIMMs w/o ECC is not a validated configuration.
5. If 1.35V & 1.5V DIMMs are mixed, the DIMMs will run at 1.5V.
6. Any combination of x8 and x16 UDIMMs, with 1Gb or 2Gb DRAM density, is supported.
7. Populate DIMMs starting with slot 0, furthest from the CPU.
8. Any combination of x8 UDIMMs, with 1Gb or 2Gb DRAM density, is supported.

3.4 Channel Population Requirements for Memory RAS Modes

The Intel Xeon processor 5600 series supports different memory RAS modes: Independent Channel Mode, Mirrored Channel Mode, and Lockstep Channel Mode. The rules on channel population and channel matching vary by the RAS mode used. Regardless of RAS mode, the requirements for populating within a channel given must be met at all times. Note that support of RAS modes that require matching DIMM population between channels (Mirroring, Lockstep) require that ECC DIMMs be populated. Independent Mode is the only mode that supports non-ECC DIMMs in addition to ECC DIMMs.

When mirrored mode is enabled and both channels are in redundant mode, if one of the channels get an address parity error, the Intel Xeon processor 5600 series is able to go into redundancy loss mode and continue operation.



3.5 Memory Error Signaling

3.5.1 Enabling SMI/NMI for Memory Corrected Errors

The MC_SMI_CNTRL register has enables for SMI and NMI interrupts. Only one should be set. Whichever type of interrupt is enabled will be triggered if:

- a DIMM error counter exceeds the threshold
- redundancy is lost on a mirrored configuration or

3.5.2 Identifying the Cause of an Interrupt

Table 3-6 defines how to determine the cause of an interrupt.

Table 3-6. Causes of SMI or NMI

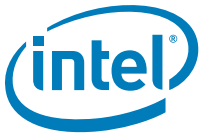
Condition	Cause	Recommended Platform Software Response
MC_SMI_DIMM_ERROR_STATUS. DIMM_ERROR_OVERFLOW_STATUS != 0	This register has one bit for each DIMM error counter that exceeds threshold. This can happen at the same time as any of the other SMI events (redundancy lost in Mirror Mode). It is recommended that software address one, so that the other cause remains when the second event is taken.	Examine the associated MC_COR_ECC_CNT_X register. Determine the time since the counter has been cleared. The counter should be cleared to reset the overflow bit.
MC_RAS_STATUS.REDUNDANCY_LOSS = 1	One channel of a mirrored pair had an uncorrectable error and redundancy has been lost.	Raise an indication that a reboot should be scheduled, possibly replace the failed DIMM specified in the MC_SMI_DIMM_ERROR_STATUS register.

3.6 DDR_THERM# and DDR_THERM2# Pin Response

Two pins are available on the Intel Xeon processor 5600 series, DDR_THERM# and DDR_THERM2#. One of the responses shown below can be configured to each pin. Existing Intel Xeon 5500 platform implementations use DDR_THERM# for the Throttling function, so DDR_THERM2# may be used for the 2X refresh function with Intel Xeon processor 5600 series. Architecturally, there is no restriction on which pin is used to control which function.

Table 3-7. DDR_THERM# Responses

Register	Parameter	Bits	One Per	Description
MC_DDR_THERM_COMMANDX	THROTTLE	1	Socket. (appears in each of the 3 channels)	While DDR_THERM# is asserted, Duty Cycle throttling will be imposed on all channels. The platform should ensure DDR_THERM# is asserted when any DIMM is over T64.
MC_DDR_THERM_COMMANDX	2X refresh	1	Socket. (appears in each of the 3 channels)	Refresh rate is doubled on all channels while DDR_THERM# is asserted. The platform should ensure DDR_THERM# is asserted when any DIMM is over T32.



3.7 2X Refresh

The Intel Xeon processor 5600 series supports 2X refresh via two mechanisms. The traditional software-based mechanism (via MC_CLOSED_LOOP register) supported on Intel Xeon processor 5500 series, and a new hardware-based mechanism (via DDR_THERM2# pin).

1. SW Based - when MC_CLOSED_LOOP.REF_2X_NOW configuration bit is set.
2. HW Based - when DDR_THERM2# pin is asserted and its corresponding MC_DDR_THERM1_COMMANDX.REF_2X register bit is set. Refer to the latest EMTS for details on the DDR_THERM# and DDR_THERM2#pins.

3.8 Pre-charge Power-Down Slow Exit

Pre-charge Power-Down Slow Exit (PPDS) is a feature of the Intel Xeon processor 5600 series which provides DIMM power savings with a small latency tradeoff. In general, PPDS is expected to be more beneficial for slower DIMM speeds (800, 1066), and the power benefit of PPDS is expected to be more significant for larger DIMMs (36 or 72 devices). System developers are encouraged to characterize their overall system power vs performance under various configurations of interest when deciding to enable PPDS. The default setting is PPDS disabled. The feature can be enabled by programming the DIMM to perform slow exit, and setting the tXP value in MC_CHANNEL_0/1/1_CKE_TIMING_B register appropriately.

Note that PPDS is *only* supported in 1DPC configurations due to complexities which arise when a powered down DIMM must terminate an access to another DIMM.

§