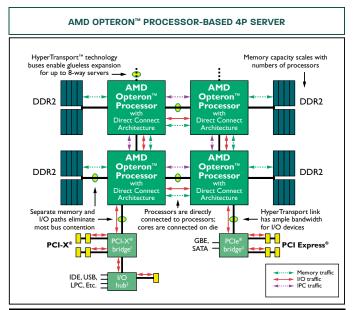
# Next-Generation AMD Opteron<sup>™</sup> Processor with Direct Connect Architecture

4P Server Comparison



## **DIRECT CONNECT ARCHITECTURE**

AMD OPTERON™ PROCESSOR-BASED SERVER

## AMD64

- » Enables simultaneous high-performance 32- and 64-bit computing
- » Delivers industry-leading performance-per-watt capabilities
- » AMD PowerNow!™ technology with Optimized Power Management provides power-on-demand computing and can help lower TCO
- » AMD's native dual-core implementation enables one platform to meet the needs of multi-tasking and multi-threaded environments, providing platform longevity
- » Hardware-assisted AMD Virtualization™ (AMD-V™) and Direct Connect Architecture provide a balanced approach to help improve virtualization performance, enabling more virtual machines to run per server

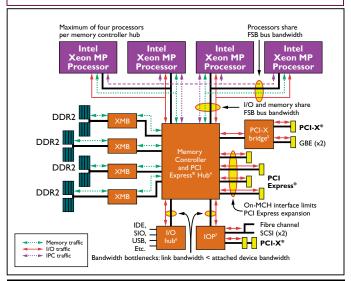
### INTEGRATED RDDR2 MEMORY CONTROLLER

- » Low latency for fast memory reads
- » Memory bandwidth scales as processors are added
- » AMD Opteron™ processors with energy efficient RDDR2 memory offer greater memory bandwidth, improved memory RAS and cost savings

## HYPERTRANSPORT™ TECHNOLOGY

» At up to 8GB/s bandwidth per link, HyperTransport technology provides sufficient bandwidth for supporting existing interconnects including Fibre Channel, Gigabit Ethernet, PCI-X,® PCI-X® 2.0, PCI Express,® Serial-ATA, Serial Attached SCSI

#### INTEL XEON MP PROCESSOR-BASED 4P SERVER



## FRONT SIDE BUS-BASED ARCHITECTURE

INTEL XEON MP PROCESSOR-BASED SERVER

## EM64T

- » Allows 32-and 64-bit simultaneous computing
- » Intel SpeedStep technology and demand-based switching
- » Hardware assisted VT must run memory-intensive virtualization applications over a shared front-side bus

## "NORTHBRIDGE"-STYLE MEMORY CONTROLLER VIA FRONT SIDE BUS

- » Passage through memory controller hub delays memory reads
- » Memory and I/O must share FSB bandwidth, further reducing the efficiency of the FSB

## MEMORY CONTROL HUB (MCH)-BASED 1/0 HUB

- » With one MCH per system, PCI Express® interface integration onto MCH limits expansion options
- » I/O hub interface can be over loaded by aggregate demands of many I/O devices
  - Intel 8501 Chinset
  - Intel 82801 EB or 82801 ER (ICH5 or ICH5R) 6700PXH

  - 10P332



AMD-8132™ HyperTransport PCI-X Tunnel

NVIDIA nForce Professional 2050 AMD-8111™ HyperTransport I/O Hub





SERVER SYSTEM COMPARISON	AMD OPTERON™ 8000 SERIES	INTEL XEON MP 7000 <sup>1</sup>
Modular, glueless scalability	Yes	Requires Northbridge
SMP capabilities	Up to 8-Sockets/16 Cores	Up to 8-Sockets/16 Cores
Direct Connect Architecture	Yes	No
Dual-Core technology	Yes	Yes
High Performance 32-bit and 64-bit computing	AMD64	EM64T
HyperTransport™ technology	Yes	No
Integrated DDR2 memory controller	Yes	No
Hardware-assisted virtualization	$AMD-V^{m}$	VT
Front side bus frequency	1800 – 3000MHz <sup>†</sup>	667/800MHz
Front side bus bandwidth	14.4 – 24GB/s <sup>†</sup>	10.6GB/s @ 667FSB; 12.8GB/s @ 800FSB
Maximum inter-processor bandwidth	8.0GB/s	10.6GB/s @ 667FSB; 12.8GB/s @ 800FSB
Memory support	DDR2 400/533/667(up to 128GB)	DDR2-400 (up to 64GB)
Memory bandwidth 4P system	42.4GB/s <sup>tt</sup>	10.6GB/s @ 667FSB; 12.8GB/s @ 800FSB
L1 cache size (max.)	64KB (Data) + 64KB (Instruction) per core	IMB
L2 cache size (max.)	1MB per core	2x 1MB and 2x 2MB
Maximum I/O bandwidth 4P system	32.0GB/s††	14.0GB/s @ 667FSB; 16.0GB/s @ 800FSB
SIMD instruction set support	SSE, SSE2, SSE3	SSE2, SSE3

DEDICATED BANDWIDTH
SHARED BANDWIDTH

- <sup>1</sup> The AMD Opteron<sup>™</sup> processor does not have a front side bus. The processor to memory controller interface is on the processor die <sup>®</sup> AMD 4P System AMD Opteron 8000 Series with 4 HyperTransport Inter-processor Buses and 4 HyperTransport I/O Buses with DDR2 667 memory.
- 667 memory

  With Intel E8501 Chipset (http://developer.intel.com/products/chipsets/e8501/index.htm)

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