IBM Global Services

Building Cell-Based Partnerships With IBM

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Why partner with IBM, and what we can do for you

- **We are creating the world's largest ecosystem and client base for high performance, commodity-based hardware**
  - Cell provides higher performance, density and power efficiency than X86 platform, FPGA accelerator or GPU-based platforms
  - Also combines Linux-based programming models that will enable a more flexible, and maintainable programming environment
- **IBM has already captured 40% of the blade server market**
  - A proven, high density form factor using open standards
- **We are projecting unprecedented compute power at commodity prices**
  - (14 blades/chassis) X (6 chassis/rack) X (2 BE's/blade) = 168 BE's
  - 168 X 200+ GFLOPS / BE = **34 TERAFLOPS / RACK**
- **Access to the IBM tech support, marketing and sales machine**
  - Joint customer selling (dedicated HPC, HW and industry sales teams)
  - Joint marketing (white papers, press, advertising, conferences)

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- technical support
- faculty grants
- loaner programs
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The Potential of the Cell Processor for Scientific Computing

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ABSTRACT

The slowing pace of commodity microprocessor performance improvements combined with ever-increasing chip power demands has become of utmost concern to computational scientists. As a result, the high performance computing community is examining alternative architectures that address the limitations of modern cache-based designs. In this work, we examine the potential of using the forthcoming STI Cell processor as a building block for future high-end computing systems. Our work contains several novel contributions. First, we introduce a performance model for Cell and apply it to several key scientific computing kernels: dense matrix multiply, sparse matrix vector multiply, stencil computations, and 1D/2D FFTs. The difficulty of programming Cell, which requires assembly level intrinsics for the best performance, makes this model useful as an initial step in algorithm design and evaluation. Next, we validate the accuracy of our model by comparing results against published hardware results, as well as our own implementations on the Cell full system simulator. Additionally, we compare Cell performance to benchmarks run on leading superscalar (AMD Opteron), VLIW (Intel Itanium2), and vector (Cray X1E) architectures. Our work also explores several different mappings of the kernels and demonstrates a simple and effective programming model for Cell's unique architecture. Finally, we propose modest microarchitectural modifications that could significantly increase the efficiency of double-precision calculations. Overall results demonstrate the tremendous potential of the Cell architecture for scientific computations in terms of both raw performance and power efficiency.

Categories and Subject Descriptors

C.1.2 [Processor Architectures] : Multiple Data Stream Architectures — Single-instruction- stream, multiple-data-stream processors (SIMD)
C.1.3 [Processor Architectures] : Other Architecture Styles — Heterogeneous (hybrid) systems
C.1.4 [Processor Architectures] : Parallel Architectures
C.4 [Performance of Systems] : Design studies, modeling techniques, performance attributes
D.1.3 [Programming Techniques] : Concurrent Programming — Parallel Programming

General Terms

Performance, Design

Keywords

Cell processor, GEMM, SpMV, sparse matrix, FFT, Stencil, three level memory

1. INTRODUCTION

Over the last decade the HPC community has moved towards machines composed of commodity microprocessors as a strategy for tracking the tremendous growth in processor performance in that market. As frequency scaling slows, and the power requirements of these mainstream processors continues to grow, the HPC community is looking for alternative architectures that provide high performance on scientific applications, yet have a healthy market outside the scientific community. In this work, we examine the potential of the forthcoming STI Cell processor as a building block for future high-end computing systems, by investigating performance across several key scientific computing kernels: dense matrix multiply, sparse matrix vector multiply, stencil computations on regular grids, as well as 1D and 2D FFTs.

Cell combines the considerable floating point resources required for demanding numerical algorithms with a power-efficient software-controlled memory hierarchy. Despite its radical departure from previous mainstream/commodity processor designs, Cell is particularly compelling because it will be produced at such high volumes that it will be cost-competitive with commodity CPUs. The current implementation of Cell is most often noted for its extremely high performance single-precision (SP) arithmetic, which is widely considered insufficient for the majority of scientific applica-

Do You Have Experience In These Areas?

Data Manipulation

- Digital Media
- Image processing
- Video processing
- Visualization of output
- Compression/decompression
- Encryption /decryption
- DSP
- Audio processing, language translation?

Graphics

- Transformation from different domains (time vs space; 2d vs 3d, viewpoint transformation)
- Lighting
- Ray Tracing / Ray casting

Floating Point Intensive Applications (SP)

- Single precision Physics
- Single precision HPC
- Sonar

Pattern Matching

- Bioinformatics
- String manipulation (search engine)
- Parsing, transformation, and Translation (XSLT)
- Audio processing, language translation?
- Filtering & Pruning

Offload Engines

- TCP/IP
- Compiler for gaming applications
- XML
- Network Security and Intrusion

Profile Of An Ideal Partner (or Client)

- **Experience in:**
  - Parallel programming models
  - Major Linux distribution
  - High performance or scientific computing applications
  - Numerics and algorithms
- **Focused on:**
  - Applications that are computationally constrained
  - Programming tools, debuggers, compilers, virtual machines, performance suites
  - Numeric libraries
  - Embedded operating systems
- **Willing to:**
  - Work with clients in identifying target applications
  - Work side-by-side with IBM to find opportunities
  - Invest time and resources in making the leap (port) to cell
  - Think creatively about novel applications
  - Open about giving us feedback on our SDK

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What Is Our Execution Timeline?